A RECONFIGURABLE OFDM MODULATOR FOR A SOFTWARE DEFINED RADIO PLATFORM

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ABSTRACT

This paper presents the development of a reconfigurable OFDM modulator based platform SDR (*Software Defined Radio*). The modulator allows operation in different modes of modulation (64-QAM, 16-QAM and QPSK) and the reuse of code. In addition it offers a good compromise between performance and area, and that it meets the reconfigurability requirements of SDR. The modulator was validated through simulation in Matlab and synthesized in FPGA device EP2C35F672C6 from Altera.

1. INTRODUCTION

The multiplicity of standards as well as the growing number of wireless communication systems have required multimode and multifunctional systems. In addition, aspects as adaptivity become more important, because they provide better quality in the received signal. These aspects have motivated the proposition and the development of highly flexible reconfigurable hardware, capable of offer the necessary flexibility and adaptability [1] [2].

Multiple carrier techniques, as OFDM (Orthogonal Frequency Division Multiplexing), represent a good solution for such systems. They, adaptability in parameters of the algorithms (number of sub-carriers, type of modulation, length cyclic prefix, etc), increasing its perfomance [1].

In this paper, we propose the design and the development of a OFDM modulator for use on SDR platform, exploiting the concepts of reuse of code and reconfigurability. The paper is organized as follows. In Section 2, an architecture proposal for an OFDM modulator is presented and the blocks are described. In Section 3, simulations and results obtained are shown. Finally, in Section 4, conclusions are drawn.

2. ARCHITECTURE

The architecture proposed is composed of three elements that define all functionalities of the system, as can be seen in Figure 1.

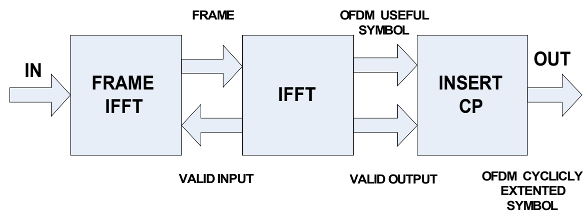

Fig. 1. Architecture proposed for OFDM Modulator.

Figure 1 summarizes not only the OFDM modulator in three functional elements, but it as also shows flow of data and communication between those elements. In the following sections the OFDM architecture will be described in detail.

2.1. Frame IFFT

FRAME IFFT Block is responsible for generation of input data set into the IFFT. Its functions include the mapping of input bits into sub-complex symbols, generation of zero padding and timing of entry. In Figure 2, we show the implemented FRAME IFFT architecture.

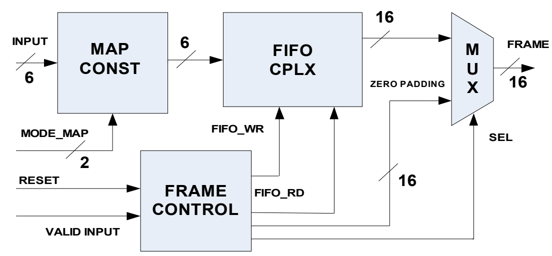

Fig. 2. Architecture of the FRAME IFFT.

MAP CONST block makes the mapping of the input bits into sub-complex symbols (QAM-64, QAM-16 or QPSK) and is also responsible for allowing the OFDM modulator to operate in different modes through *mode_map* signal. Moreover, modulation mode can be changed in real time without loss of the OFDM signal processing. This block is composed of single memory complex ROM, instead of one for each type of modulation used [3], being adequately addressed by an internal unit called CONF MAP.

FIFO CPLX is responsible for storing the mapped data for later reading. The MUX makes the selection between mapped data and zero paddings generated by FRAME CONTROL and, together with FIFO CPLX, helps in formation of the frame of input IFFT.

FRAME CONTROL block is responsible for all dynamics of the IFFT frame and for generation of the zero paddings. The blocks of the IFFT FRAME are described in a generic way, allowing the implementation of different configurations for modulator.

2.2. IFFT

IFFT is the principal component in computation of the OFDM symbol, being responsible for the generation of N orthogonal sub-carriers. This block implements radix 2 IFFT of length 16 in fixed-point arithmetic. The architecture of IFFT is based on memory and is composed for unit of processing, two dual port RAM memory (one for processing and another to store the data output), a memory ROM, address generator unit and another for controller processor. Figure 3 show the architecture of IFFT.

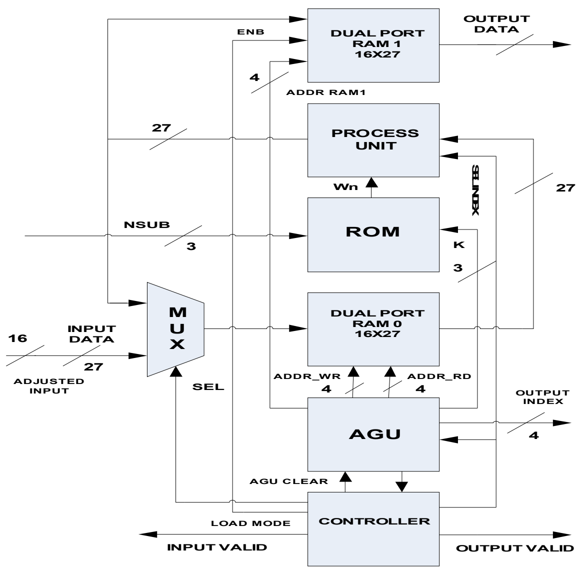

Fig. 3. Architecture of the IFFT.

The reason for choice the architecture based on memory is same allow to overlap the operations of input and output of data to the processing. While RAM0 is used in processing of an IFFT, RAM1 is used in operation of output from the previous IFFT. In the last stage of processing, RAM0 receives new data entry, processing concurrently with the last stage, while the result of IFFT is written in RAM1 and then sent in serial form. This represents a considerable reduction in latency in the processing of IFFT. The RAM0 and RAM1 memories addition to performing basic tasks of processing and storing of data, has conversion feature series-parallel and parallel-series, respectively.

The RAM0 receives the frame of data in serial form, storing them to be processed subsequently held every butterfly, while RAM1, stores samples of useful OFDM symbol, and provides a way serial. PROCESS UNIT is responsible for IFFT arithmetic. This unit carries data from the RAM0, computes a butterfly stage of the IFFT and returns the result of the calculations to the same address from where the data was previously extracted.

AGU (Address generator Unit) is responsible for generation of the addresses of reading and writing of memories RAM0 and ROM and operations entry and output of data. These addresses are referenced as index0, index1 and k. AGU implements a block called SKEW which have function to place the addresses index0 and index1 of a sequence of reading and writing appropriate for the output *addr_wr* and *addr_rd*.

ROM memory stores the complex exponentials functions that define orthogonal sub-carriers. This block is configurable and allows operation of the IFFT with different lengths of N, with the signal *nsub*.

CONTROLLER is responsible for all dynamic processing of the IFFT and by providing the signals *input_valid* and *output_valid*, which serve as indicators of control for the FRAME IFFT and INSERT CP in timing output and entry of data modulator. MUX input is responsible by selecting between the input data and the partial results sent to IFFT RAM0 memory. The data circulating in buses shown in Figure 3 are complex, so there are actually two buses in parallel, being real part and other for imaginary part of the signals. The components of the IFFT also are implemented in generic form applying the concept of reuse of code.

2.3. Inserted Cyclic Prefix

INSERT CP is the block responsible for insertion of the cyclic prefix in the formation of OFDM symbol cyclically extending and in the timing of output data. In Figure 4, the architecture of INSERT CP is illustrated.

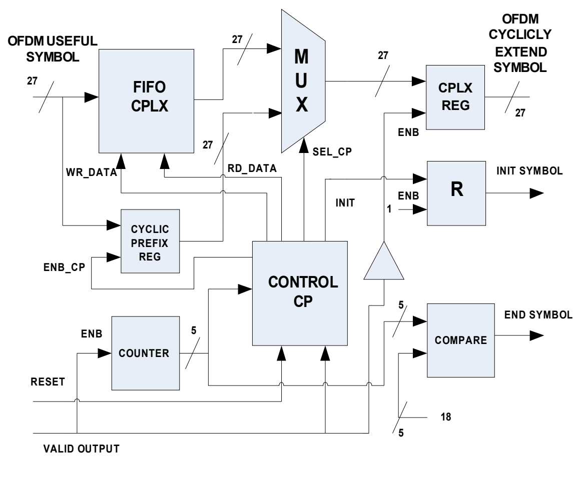

Fig. 4. Architecture of INSERT CP .

The block FIFO CPLX is responsible by storing samples of useful OFDM symbol (results of IFFT) for later reading. The CYCLIC PREFIX REG stores the cyclic prefix for its later reading. MUX does the selection between the samples of a useful symbol OFDM and cyclic prefix stored in the register.

CONTROL CP defines each step in the formation of the OFDM symbol cyclically extending and establishing the timing of output of the modulator. As FRAME IFFT and IFFT, the blocks of INSERT CP also are implemented in generic form, allowing reuse of code.

3. SIMULATIONS AND RESULTS

For realization of tests, OFDM modulator was described in Matlab as theoretical reference for valuation of model in VHDL detailed in Section 2. Right away the modulator was synthesized in FPGA EP2C35F672C6 from Altera. The specifications of modulator are shown in Table 1 and the synthesis results in Table 2. After a pseudo-random sequence was generated and submitted in both models of modulator. During tests, the modulator is configured for modulations QAM-64, QAM-16 and QPSK. In output, the results obtained are observed and compared. The wave forms obtained from synthesis in FPGA are plotted with help of Matlab tool as show the Figures 6, 7 and 8.

In this figures, the spectrum of OFDM signals is shown for different modulations (QAM-64, QAM-16 and QPSK) together with its the respective constellations. The OFDM signals have 16 sub-carriers, where only eight sub-carriers carry information as shown in Table 1. Results show the spectrum's of OFDM signal for modulations evaluated are coherent with the results measured theoretically in Matlab and demonstrates functionality of system implemented. The peaks present in OFDM signal are attributed to the level DC introduced in each sub-carriers by train of pulses in entry of modulator. These peaks can be eliminated with use of simple filter low pass or through of the use of technique windows as raised cosine.

The modulator was validated experimentally for Cyclone II EP2C35 DSP development board which has FPGA EP2C35F672C6 and a converter D/A of 14bits with 165MSPS capabilities in output. However, the results not were satisfactory due to absence of filter in output of modulator to eliminate a level DC and and because of that was not shown.

Table 2 shows modulator demands few logic resources of FPGA and present maximal clock frequency of 80.34MHz. The frequency of operation is not more high due to IFFT block which limit the speed in comparison to the blocks FRAME IFFT and INSERT CP which can to operate with frequency of clock of order 235MHz. Also theoretically are measured to the bit rate for each type of modulation showed in Table III.

Device	EP2C35F672C6 da Altera
Length of Frame	16
Length of IFFT	16
Number of sub-carriers	16
Number of Mapped Data	8
Number of zero paddings	8
Length of Prefix Cyclic	4
Frequency operation	50MHz
Bandwidth	25MHz
Sub-channel	3.125MHz
Means time for generation of OFDM symbol	1.28μs
Interval of useful symbol	0.32μs
Interval of OFDM symbol cyclically extended	0.4μs

Tab. 1. Specifications of the OFDM modulator.

Logic elements	715 (2%)
Combinational functions	645 (2%)
Registers	395 (1%)
Pins	166 (35%)
Memory bits	2848 (<1%)
Multipliers of 9 bits	16 (23%)
Maximal frequency of operation	80.34MHz

Tab. 2. Resources required by OFDM modulator.

Type Modulation	Rate
QPSK	40Mbits/s
QAM-16	80Mbits/s
QAM-64	120Mbits

Tab. 3. Bit rate measured.

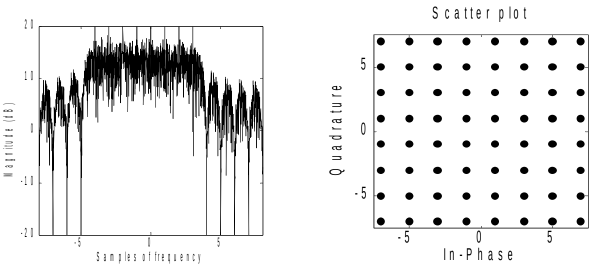

Fig. 6. (a) OFDM spectrum of the signal for QAM 64 modulation. (b) Constellation QAM-64.

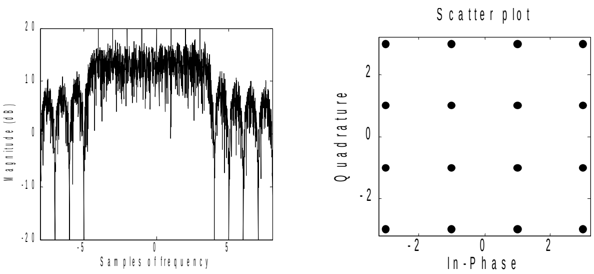

Fig. 7. (a) OFDM spectrum of the signal for QAM 16 modulation. (b) Constellation QAM-16.

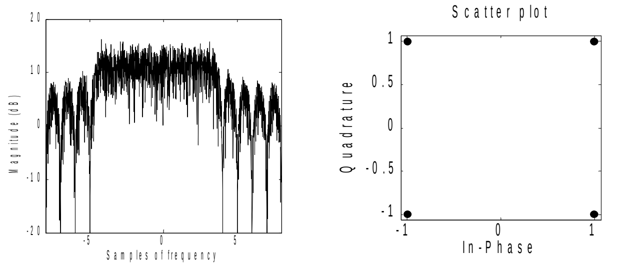

Fig. 8. (a) OFDM spectrum of the signal for QPSK modulation. (b) Constellation QPSK.

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4. CONCLUSIONS

In this work, was presented the design and development of OFDM modulator for on SDR platform. It was shown that modulator is reconfigurable, allowing the application of different modulations in real time with *mode_map* signal. It was also shown that the solution applies the concept of reuse of code, allowing different settings. The solution allow also reconfigures the number of sub-carriers from the restart of the modulator. In future work, seek to develop a fully reconfigurable OFDM modulator based on the SDR.

5. REFERENCES

[1] Gerard K. Rauwerda, Paul M. Heysters, and Gerard J. M. Smit, "Towards Software Defined Radios Using Coarse-Grained Reconfigurable Hardware", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, VOL. 16, NO. 1, January 2008.

[2] Qiwei Zhang, Andre B. J. Kokkeler and Gerard J. M. Smit, "Adaptative OFDM System Design For Cognitive Radio", Proceedings of the 11th International OFDM-Workshop 2006, Hamburg, Germany.

[3] James Veilleux, Paul Fortier and Sébastien Roy, "An FPGA Implementation of an OFDM Adaptive Modulation System", NEWCAS 2005.

[4] U. S. PATENT 3,488,445 – "*Orthogonal Frequency Division Multiplexing",* Filed Nov. 14. 1966, issued Jan. 6, 1970.

[5] S. B. Weinstein and Paul M. Ebert, "Data Transmission by Frequency-Division multiplexing Using the Discrete Fourier Transform",*IEEE Transactions on Communication Technology*, VOL. COM-19, NO. 5, October 1971.

[6] Pinto, Ernesto Leite e Albuquerque, Cláudio Penedo, "A técnica de transmissão OFDM", *Revista cientifica periódica - telecomunicações*, v.5,n.1, jun. 2002.

[7] Chris Moffatt and Anders Mattsson, *"Computationally Efficient IFFT/FFT Approximations for OFDM",* Military Communication Conference – MILCOM 2007, Harris Corporation, Melbourne, FL, in 2007.

[8] Steve Gifford, John E. Kleider and Scott Chuprun, "*Brodband OFDM Using 16-Bit Precision on a SDR Plataform*", Integrated Information System Group Motorola., Scottsdale, Arizona, USA.