FULL-ADDER DESIGN USING QUANTUM-DOT CELLULAR AUTOMATA LOGIC GATES

Manoel F. de Queiroz Neto , Fernando Rangel de Sousa

μEEs/DEE/CT – Federal University of Rio Grande do Norte,
Campus Universitario, Lagoa Nova ,59072970, Natal – RN, Brasil
Phone:+55-84-32153910, Email ee.neto@yahoo.com.br , rangel@ieee.org .

ABSTRACT

This work presents the design and simulations results of a full adder using the Quantum-dot Cellular Automata (QCA) technology. This technology is a molecular computing, which represents the binary information using the charge configuration of quantum dots. The paper shows the main design of properties of QCA cells, the universal design logic gates and the design a full adder using these gates. These designs were made by QCA*Designer* software.

1. INTRODUCTION

With the large increase in the capacity of producing even smaller devices and the associated difficulties, many technologies in the nanometer scale are begin investigated. Among them, Quantum-dot Cellular Automata (QCA) is currently gaining popularity as a future replacement for the transistor [1]. It was first proposed in 1993 by Lent, et. al and fabricated in 1997.

Recently, several studies have been done involving QCA, using the QCA*Designer* [2] software. The QCA*Designer w*as designed at the ATIPS Laboratory, University of Calgary, to create a designs and to simulate Quantum-Dot Cellular Automata (QCA) applications.

The purpose of this paper is to show that any digital circuit (in specific the full adder) can be designed with QCA cells through the use of universal logic gates. It will also show the design of a full adder of one bit, using the logic gates XOR, AND e OR.

2. PROPERTIES OF QCA CIRCUITS

Quantum dots are nanostructures created from standard semiconductor materials, such as InAs/GaAs. These structures can be modeled as 3-dimensional quantum wells. As a result, they exhibit energy quantization effects even at distances several hundred times larger than the material system lattice constant. Electrons, once trapped inside the dot, do not alone possess the energy required to escape. The QCA cell is defined as a junction of four quantum dots arranged in the shape of a square, so that two moving electrons are isolated within the cell. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic repulsion.

As a result, they can assume two positions in diagonals, which can be encoded in binary through defining these positions as polarization -1 and +1, assuming logic values 0 and 1 respectively [3]. (Figure 1)

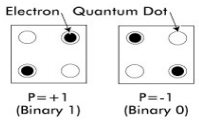


Figure 1 . The geometry of the two QCA cells created with four quantum dots located at the vertices of the square. The cell is charged with two free electrons that tend to occupy the diagonal. The two cells are in different polarizations (P= +1 and P= -1).

Since the electrons are quantum mechanical particles, they are able to tunnel between the dots in a cell. The electrons in cells placed adjacent to each other, will interact. As a result, the polarization of one cell will be directly affected by the polarization of its neighboring cell, assuming this polarization. If placed in diagonal, instead of the cell assuming the same polarization of the neighbor, it will have the opposite polarization [4]. (Figure 2)

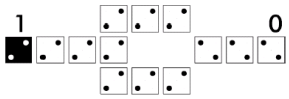


Figure 2. The inverter. The cells are placed on diagonal.

The software QCA*Designer* also allows placing the quantum dots of a normal cell (in which the dots are placed in the shape of a square) in vertical-horizontal positions, so that if there is an information flow through normal cells, it can cross another information flow via vertical-horizontal cell, as if they were a wire going

above the other (without interference occurrence) (Figure 3). However, the difference of vertical/horizontal cells is that instead of getting the same polarization of its neighbor (normal cells); they get the reversed polarization [5].

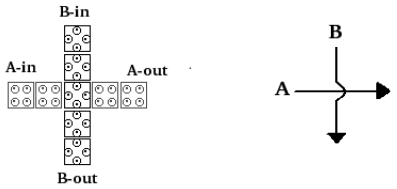
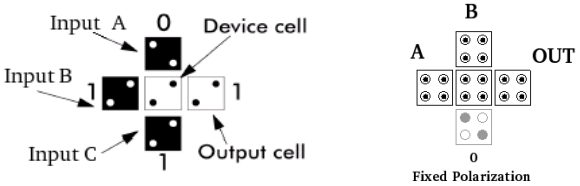


Figure 3. The crossover of QCA's wires. The information flow has no interference.

The information that passes through a wire on vertical-horizontal cells can be caught and passed to normal cells. So it requires placing a normal cell on top of the two cells vertical-horizontal, as shown on input "A" in figure 6.a). Since the vertical-horizontal cells assume the reverse polarization of its neighbor, it can catch the normal information or reversed, depending on where the normal cell is placed. This feature can be used to model a NOT gate. The NOT gate can also be model as shown in figure 2. Other important characteristic is the majority gate, in which the information flow that passes to the OUT will be the majority.(Figure 4.a))



4 a) Majority gate 4 b) AND gate

Figure 4. a) Majority gate. The information that will appear in the output is the majority of the inputs. b) By fixing the polarization of one input (input c) as logic "1" or "0", it can be obtained an OR gate and an AND gate respectively.

In the QCA's software, there are four different clocks, delayed 90 degrees each, which are used to control the information flow in cells. The cells are active (moment that they get any polarization) or inactive (the polarization is zero) depending on the zone of clock that it was in [6] Figure (5).

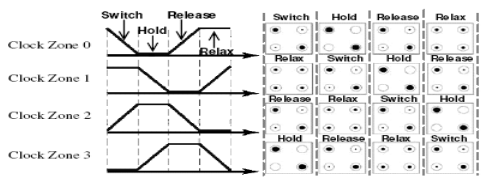


Figure 5. The four clock zones. When the clock signal is low (hold), the cells are latched. When the clock signal is high (relax), the cells are relaxed and have no polarization.

3. DESIGN OF QCA LOGIC GATES

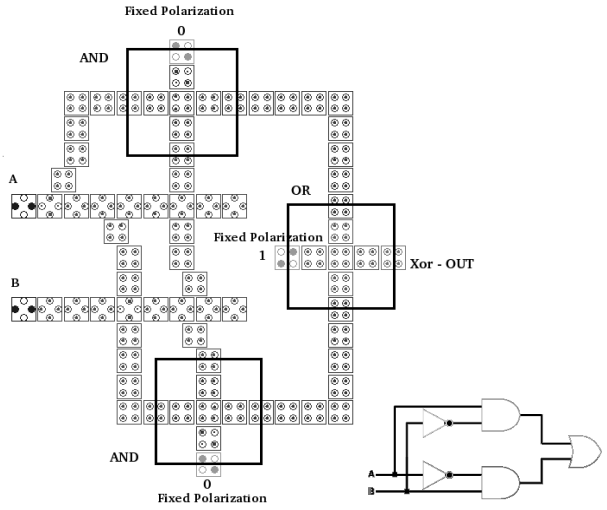
As exposed above, using the software QCA*Designer* , it is possible to design and simulate logic gates, full adders, memories, and several types of digital circuits.

With QCA*Designer,* the properties of the QCA cells and the logic gates AND (figure 4.b)), OR, NAND, NOR, XNOR, XOR (figure 6) were designed and simulated. In figure 7 is shown the simulation results of a XOR gate. When the clock is low, the cells are lacthed and behave as a XOR gate.

The XOR gate is formed with two AND gates, one OR and two inverters. Through the combination of these gates, it is possible to implement the full adder. However, to form the full adder (Figure 9) it is required the use of the half adder (Figure 8), which is formed by an AND gate and a XOR gate [7]. The full adder shown in this paper sums the inputs (A, B, "carry in") bit by bit and generates two outputs ("carry out", OUT). (Figure 10.c)

The inputs "A" and "B" are connected to the first XOR. The output of this XOR and the "Cin"(carry in) are connected to the second XOR (the output of this XOR is the sum of "A" and "B"). "A" and "B" are connected to the first AND and "Cin" with output of first XOR, connected with the other AND. The outputs of ANDs are connected with the OR, and its output is the carry out.

By connecting the "carry out" of one full adder in the "carry in" of the other, it can be obtained as a result the full adders to sum numbers with n Bits.



6. a) 6. b)

Figure 6. a)The XOR gate of QCA cells, made with two ANDs gate and one OR. A and B are inputs. b) The digital XOR gate with logic gates.

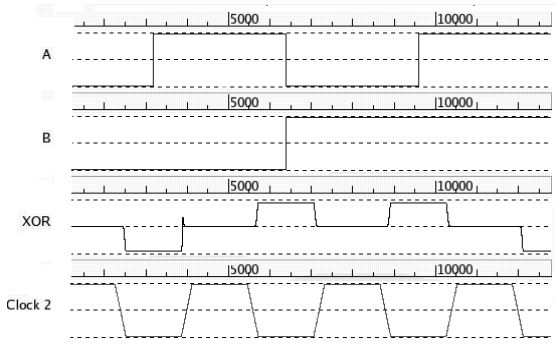


Figure 7. Simulation of a XOR gate. A and B are vectors of inputs and the output is XOR.

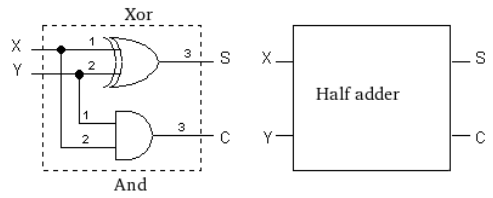


Figure 8. The half adder [8], constituted of one XOR gate and one AND gate.

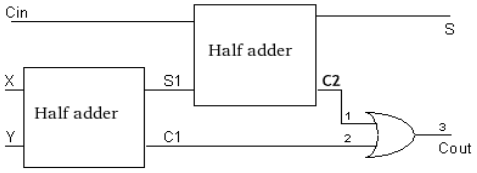


Figure 9. The full adder [8], constituted of two half adders (two XOR and two AND) and one OR.

X	Y	Cin	Sum	Cout
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Figure 10. a) The truth table of the full adder. The output "Sum" represents the sum of the inputs, and "Cout" represents the carry out.

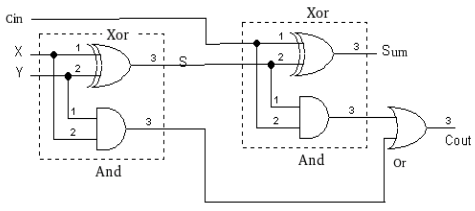


Figure 10. b) Schematic of digital full adder.

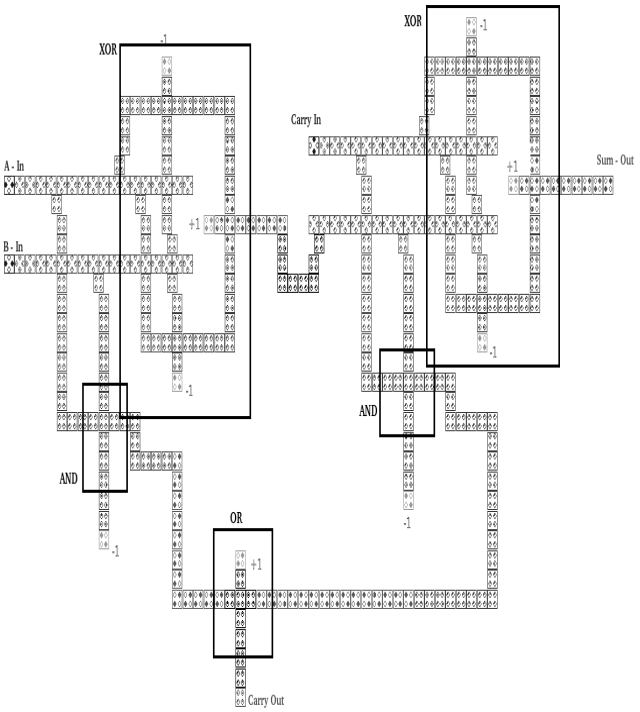


Figure 10 c). The full adder of QCA cells. It is formed by two XOR gates, two AND and one OR.

4. CONCLUSION

In conclusion, with the software QCA*Designer* and based on the characteristics of QCA cells, the design of a full adder (Figure 8.c)) using logic gates (two XOR, two AND and one OR) was developed.

Besides studies concerning full adders, there are several other researches that can be made in the same direction, such as: recorders, multiplexers, ALU [8], memories, drivers, microprocessors, etc.

It is clear that the QCA technology, which is implemented in nano-scale, has great potential, considering it is much smaller and faster than the transistor. Also, QCA cells can form any digital circuit through the universal logic gate, becoming a possible replacement for the transistor in the future.

It is important to mention, however, that the QCA cells are very unstable and suffer great influence by temperature and by other problems. If these problems are solved, this technology will make a strong impact on technological advance, allowing smaller and efficient processors and electronics and providing many improvements in human life.

5. ACKNOWLEDGMENTS

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