A RECONFIGURABLE MC-DS-CDMA DIGITAL TRANSMITTER FOR SDR MOBILE TERMINALS

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ABSTRACT

It is only a matter of time before software defined radio (SDR) technology reaches mobile and handset terminals. Therefore, the necessity for the hardware to be able to adapt to the conditions set by the new wireless technologies, such as 4G wireless systems, will become the main challenge to overcome. Flexibility will be a key factor for the implementation of such complex wireless systems. Hence, the purpose of this paper is to describe the design and implementation process of the base band and IF (intermediate frequency) stages of a flexible multicarrier CDMA (Code Division Multiple Access) transmitter on a FPGA (Field Programmable Gate Array). Likewise, it is the main objective of this paper to highlight the benefits of the architecture implemented that make it ideal for the SDR technology.

1. INTRODUCTION

Reconfigurability has been an important issue for communication systems since the beginning of the new millennium. As a result, SDR technology has been the one to emerge as the most ideal solution for the realization of multi-standard radio stations. The future wireless technologies will demand highly flexible hardware in order to meet their very complex requirements, such as Multi-Protocol Applications and Dynamic Spectrum Access [1].

SDR technology establishes that certain parameters – such as the frequency band, bandwidth, modulation and coding schemes and so on – must be reconfigurable in order to change the behavior of the communication system [2]. Since software interfaces are the most user-friendly like, the hardware must be able to get the information from the software and then perform the corresponding changes. One of the most preferred alternatives for the implementation of the base band stage in hardware is the use of a DSP (Digital Signal Processor) [3] with special resources that target high speed signal processing. However, the high bit rates and the speed demanded by SDR technology cannot be reached by these devices. Hence, the available alternatives are FPGAs, ASICs (Application Specific Integrated Circuits), or even SOCs (Systems on Chip) if portability, in terms of really small sizes, is required.

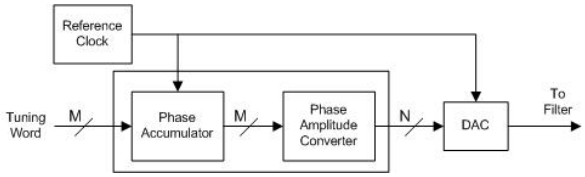

Figure 1. Scheme of a Direct Digital Synthesizer.

Due to the fact that SDR technology has been developed for wireless systems, not all modulation schemes need to be implemented. CDMA is one of the most popular in cellular systems and wireless networks; hence, the importance of efficient and flexible CDMA transceivers [4].

This article explains the design and implementation of an electronic device that performs a Multicarrier - Direct Sequence – CDMA algorithm that allows you to choose the number of carriers and the Spread Factor, as well as the frequency of each subcarrier. This digital system was implemented on the Cyclone II FPGA, for circuit emulation purposes. Nevertheless, it is important to highlight that this is not the final implementation of the system. The final goal of this research is to implement the VLSI architecture of the system for the future SOC.

Implementations of CDMA transmitters on FPGAs have already been done, for both dedicated and reconfigurable hardware. However, most of them target the already exiting applications, where voice transmission over cellular networks stands out from the rest [5]. Therefore, all the requirements involved with this particular service has a significant influence with the goals set for the sought device; for instance, there is no concern whatsoever about working with high data bit rates, and designing circuits that induce a very low amount of latency, since digitalized voice has data bit rates in the order of Kbps. Nevertheless, it is one of the main objectives of this paper to present an architecture that could adapt to the new wireless technologies, which implies setting high goals for the performance and efficiency of the implemented device.

This paper is divided in four different sections: the first one describes the foundation of DDS (Direct Digital Synthesis); the second one describes the architecture undertaken; the third one gives the details of the results obtained from the implementation stage; and the fourth one gives the final conclusions.

2. DIRECT DIGITAL SYNTHESIS

DDS techniques are becoming more common within digital communication systems that work with sinusoidal carriers. The ability to generate multiple frequencies from only one clock signal [6] comes in handy for reconfigurable communication systems (variable carrier frequency), such as the ones required for SDR devices. The objective for DDS techniques is to implement an NCO (Numerically Controlled Oscillator) that allows us to set the frequency of the output signal. The core of the DDS scheme, depicted in Figure 1, is the phase accumulator, which is basically a phase wheel that represents all 360 degrees. With every rising edge of the clock it goes up one position inside the phase wheel until an entire lap is completed. Then the process repeats itself all over again, which make it similar to the periodical feature of a sinusoidal wave. Nevertheless, it is important to clarify that the increment is set by the Tuning Word signal, which has a word length of M bits. Thus, we are able to vary the frequency by changing the Tuning Word value. The equation that determines the frequency of the output signal is expressed as

$$f_o = \frac{M \times f_{clk}}{2^n} \qquad (1)$$

In (1), the f_o variable represents the frequency of the output signal; the M variable represents the Tuning Word signal; the f_{clk} variable represents the clock frequency; and 2^n represents the number of points inside the phase wheel. So, it is clear to see that the more points inside the phase wheel, the more accuracy in the yielded signal by the DDS. The output of the Phase Accumulator becomes the memory address (M-bit word) of the Phase Amplitude Converter (sine lookup table). The numeric values stored inside the lookup table are sent to the DAC (Digital to Analog Converter) in an orderly fashion in order to shape the sinusoidal wave [7]. Ultimately, it is necessary to smooth the signal and eliminate its spurious components. The allocation of a Low-Pass Filter is thus mandatory for an appropriate generation of the carrier.

3. ARCHITECTURE AND OPERATION

Though most CDMA implementations comprise different types of spreading factor codes, such as walsh, gold, kasami and so on, the one undertaken here uses only orthogonal codes. What driven the design of this system to this apparent lack of versatility – in terms of null cross-correlation spreading codes – is that most likely each subcarrier will have a unique frequency allocation [8]. Therefore, a null cross-correlation, such as the one provided by random codes, will not be essential. Hence, the selection of a much simpler, implementation-wise, but equally effective set of

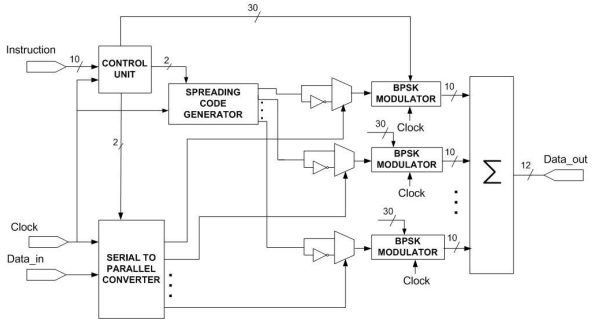

Figure 2. Scheme of the MC-DS-CDMA Transmitter.

spreading codes: OSVF (Orthogonal Variable Spreading Factor).

The data comes in a serial stream and is divided into several subcarriers. The number of subcarriers used by the system is set by the instruction signal. This signal enters directly the Control Unit, which is in charge of interpreting the opcode (operation code) of the instruction and configure all of the others functional units of the system. With every rising edge of the clock, the Control Unit refreshes the register that stores the instruction signal in order to make the appropriate changes.

Both the Serial to Parallel converter and the Spreading Code Generator receive the same two-bit word from the Control Unit, as it is shown in Figure 2. This control signal sets the number of subcarriers required, which is also the spreading factor. After the number of subcarriers is set, the data has to be multiplied by its corresponding code, mathematically speaking. Nevertheless, since a '0' value of the data involves an inversion of the spreading code, the design of the hardware had to follow another approach different from an actual multiplier. The use of a multiplier implies more latency of the circuit, more area used and more power consumption. Furthermore, it would be necessary to make the multiplier work with integer numbers, both positive and negative, which makes the implementation a lot more complex. Hence, we needed a much simpler and faster way to perform the theoretical multiplication. Since multiplexers have always been reliable and fast sources for circuit design, we design the multiplication stage based on one. The spreading code is divided into two equal streams. One of this streams passes through a NOT logic gate, and then enters the multiplexer along with the non inverted signal. Due to the fact that the data is the one that determines whether or not to invert the code, each subcarrier becomes the selector of its corresponding multiplexer.

What comes out of each multiplexer enters a BPSK (Binary Phase Shifting Keying) modulator, where the frequency allocation is selected by the Tuning Word signal. The Control Unit sends a 30-bit word (Tuning Word) to each BPSK modulator in order to set the NCO located within.

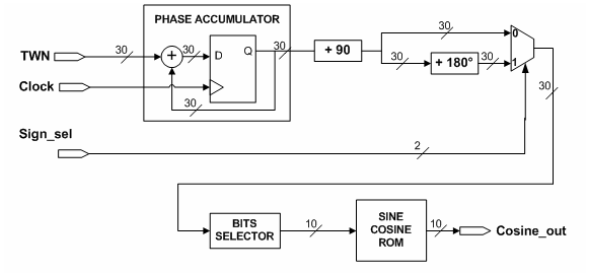

Figure 3. Scheme of the BPSK Modulator.

Finally, all of the modulated subcarriers are added together before they are sent to the DAC. Before sending it to the DAC, it would be best to pass the signal through a load stage in order to eliminate all spurious components that comes from wrong data and glitches of the circuit. The load stage would perform a synchronization task as well.

3.1. Spreading Code Generator

This functional unit receives as parameters the 200 MHz clock signal of the development board, and the spreading factor, which is a two-bit word driven by the Control Unit. Each of the following values: "01", "10" and "11, corresponds to a spreading factor of 2, 4 and 8, respectively. When this two-bit word takes the value of "00", the Control Unit disables the whole unit for low power consumption purposes. Those three values will also be the same as the number of available outputs of this stage, which is also the division factor of the data after the serial to parallel converter. The noise signals are based on OVSF codes, which are stored in registers. A general multiplexer, that has as selector the spreading factor signal, distributes all the orthogonal codes from the registers to the 8 outputs.

3.2. Control Unit

The opcode that this unit receives as input can be divided in two parts. The first two bits are the spread factor, which sets the number of division made to the data in the serial to parallel converter, and the number of spreading code outputs. The other 8 bits represents the desired frequency for the BPSK modulators. As it is shown in the Figure 2, the 30-bit word output from this unit corresponds to a float format of this frequency, for precision improvement. Since there is a limited number of choices for the selection of the frequency, it is necessary to set only one Tuning Word signal (30-bit word) and calculate the other ones required based on the first one. Thus, we are able to manage a wide a range of frequency bands and allocate the spectrum based on the frequency assigned to only one subcarrier.

Due to the fact that an 8-bit word provides only 256 possibilities, the frequency range must be constrained in order to fit the finite number of options. Therefore, the lowest and highest limits of the frequency were set to 12.5 MHz and 50 MHz respectively.

3.2. BPSK Modulator

BPSK modulation has always been one of the main stages of any kind of CDMA implementation. It basically consists on a two point constellation that only establishes whether or not to invert a cosine wave depending on the base band signal. Hence, the DDS theory is ideal for the implementation of this functional unit.

The architecture of the implemented DDSs, depicted in Figure 3, shows the simplicity and flexibility of the subsystems. The main functional unit of this subsystem is the Phase Accumulator. This stage receives the clock and the TWN –Tuning Word assigned to the N sub-channel – signals and goes through the entire count. Seeking less hardware and power consumption, this unit was implemented with one Flip-Flop D with a feedback loop. With every rising edge of the clock, the TWN is added to the value of the count [7]. The output of this stage is added with a delay of 90 degrees in order to obtain the cosine signal. The actual inversion of the signal is done after the stage of the Phase Accumulator and the 90 degrees phase delay. The data that enters the modulator acts as a selector for a 2x1 multiplexer, which has as input signals both the inverted and the non inverted signal.

The sine/cosine ROM functional unit receives only the 10 MSBs of the previous signal for low latency purposes [7]. If the address signal is represented by a large number of bits, the time that is necessary to find the corresponding value inside the memory will increase, which is detrimental for this kind of circuits that are intended for fast signal processing. Moreover, the width of the values stored inside the memory is set by resolution of the DAC available for the implementation. In this particular design, a 10-bit DAC was selected for the system.

4. IMPLEMENTATION AND RESULTS

The reconfigurable MC-DS-CDMA Modulator was implemented on the cyclone II FPGA, specifically EP2C35F672C6. It used 1038 LEs (Logic Elements), 1 embedded PLL for the generation of the 200 MHz clock frequency, and 1 ROM, and works within the following frequency range: [12.5 - 50] MHz. The center frequency selected for the testing stage was 40 MHz. The device was configured to use all 8 subcarriers and it was designed to work with an input data bit rate of 100 Mbps. It might seem unusual that a CDMA transmitter works with an input data bit rate as higher as 100 Mbps; however, due to the fact that this circuit was designed for the future 4G wireless networks (cellular networks based on IP packet switching), such high bit rates will become a requirement for the future transceivers. Hence, designing a device that could work at such a high speed was one of the main goals of this research. Moreover, it is important

to mention that this circuit takes four clock cycles – equivalent to 20 ns – to generate the MC-DS-CDMA signal, which is also a great achievement for the research.

Since the development kit did not posses a high resolution DAC, it was necessary to find another way to verify the right performance of the circuit. With the simulation tool Quartus II Web Edition of the Altera Company it was possible to identify the sequence of values – expressed as 12-bit words – provided by the CDMA transmitter. That sequence was used in a script edited in the Matlab software, where we could simulate the digital to analog conversion. In addition to that, Altera's simulation tool made it possible to observe an approximation of the behavior of the real circuit, where it was possible to identify the latency induced by the very circuit, which ranges from 5 to approximately 12 ns.

The simulation result of the Matlab script is shown Figure 4, where it is clear to see 8 peaks that represent each subcarrier and gives an estimate of 60 dBc (SFDR: Spurious Free Dynamic Range).

This implementation appears as a much faster and more efficient solution compared to previous ones, such as the CDMA transmitter described in [5], where the circuit takes 17 μs to perform the modulation. Nonetheless, it must be clarified that the benefits supplied by this architecture are counteracted by a substantial increase of the circuitry involved, which will manifest as more area and power consumption of the final integrated circuit.

5. CONCLUSIONS

The Reconfigurable MC-DS-CDMA Digital Transmitter has been presented. The benefits reached by DSPs on FPGAs or ASICs clearly surpass those provided by PDSPs , due to the fact that the former comprises a high level of parallelism ideal for SDR technology. Furthermore, DSPs implemented on FPGA or ASICs are able to attain higher data bit rates and to execute the signal processing algorithms at an acceptable speed for Real Time applications.

Whether you use the FPGA for the final implementation or as an emulation tool, it will always be an important stage of the design flow of complex communication systems such as the one undertaken on this paper. Hence, HDL (Hardware Description Language) codes, most likely, will remain as the main tool for logic design of the base band and IF stages of SDR devices.

This Reconfigurable CDMA Digital Transmitter supplies maximum flexibility and a high quality signal and represents a good starting point for deeper research in the area of SDR and CR (Cognitive Radios).

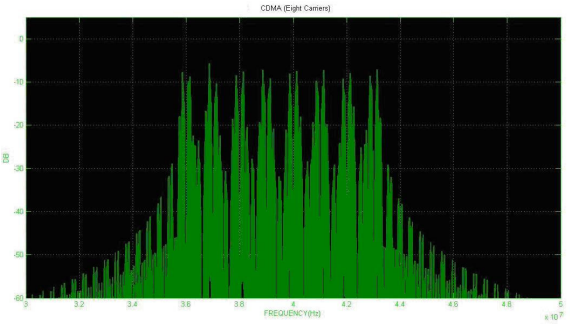

Figure 4. Spectrum of the generated CDMA signal.

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