SIMULATION AND PARAMETER EXTRACTION OF CMOS DEVICES

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ABSTRACT

The parameter extraction of CMOS devices finds a wide set of applications and interests in microelectronic industry. Essentially, this work presents methods used for simulation and parameter extraction of CMOS devices, such as mathematical analysis and computer simulation. The mathematical analysis is based on graphical studies of the current, tension and capacitance curves of the measured components. Then, with the variables available several parameters are extracted through mathematical equations. The computer simulation is performed by the software *Advanced Design Systems* (ADS). Due to its wide capability to optimize parameters, the ADS allows the user to obtain these parameters through iterative simulations, until the desirable error is reached.

1. INTRODUCTION

In this work, the electrical and capacitance measures were obtained from transistors and capacitors made in CCS, using the equipment Kethley 4200SCS. The measures were performed through needles positioned on the terminals of the components, and the data are stored in output files.

The researches Hugo Ricardo Jimenez Grados, Angélica Denardi de Barros and Juliana Miyoshi have gently provided the measures of their components.

2. MATHEMATICAL ANALYSIS

The mathematical analysis were based on the results obtained from Grado`s nMOS transistors. The main characteristic of these components is the deposition of Si-Ge on gate terminal, which it makes them suitable for RF applications. All of them share the same drain and bulk terminals, and therefore the width channel (W) is equal to 20μm [1].

2.1. Maximum transconductance

The first parameter to be evaluated was the maximum transconductance, whose value can be determined by differing the I_D x V_{GS} curve according equation (1), where I_D and V_{GS} are respectively the drain current and gate voltage [2].

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=0.1V} \qquad (1)$$

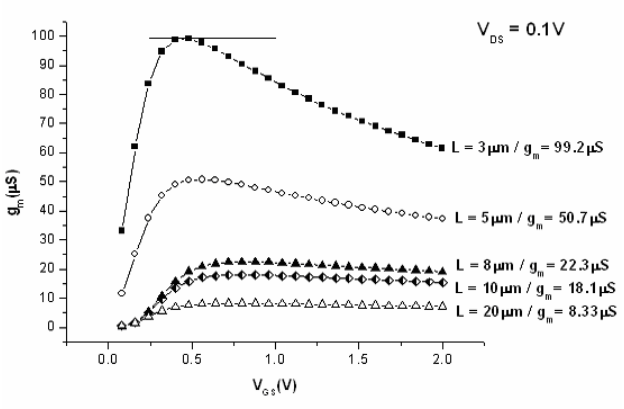

Figure 1. Transconductance curves of nMOS devices.

Figure (1) shows the transconductance curves of different transistors of the wafer, with their respective length channel (L) and maximum transconductance. The drain voltage (V_{DS}) had a constant value of 0.1V.

2.2. Electron mobility

With low constant values of V_{DS}, it is possible to describe a linear relationship among the conductance and the width and length channel, when the transistor is operating in linear regions of V_{GS}. However due the imperfections in lithography and corrosion processes, as well as the lateral diffusion of dopants, the effective length channel (L_{ef}) is the result of the reduction of length channel mask (L_M) by a factor ΔL [2].

$$L_{ef} = L_m - \Delta L \qquad (2)$$

From equation (2) we obtain the equation (3), where C_{OX} is the capacintance per unit area and μ_N is the electron mobility:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W.C_{OX}.V_{DS}}{L_{ef}}.\mu_N$$

$$\frac{W}{g_m} = \frac{1}{C_{OX}.V_{DS}.\mu_N}(L_m - \Delta L) \qquad (3)$$

The factor ΔL can be found by intersection between the curve with the horizontal axis, and according to Figure 2 its value was 1.5459μm.

The next parameter found was the capacitance C_{OX}. In this work, we calculated it by the ratio between the capacitance in accumulation region and its area [2]. Figure 3 shows the capacitance curve of a retangular CMOS capacitor in the same wafer. The capacitance C_{OX} was 4,525fF/μm^2.

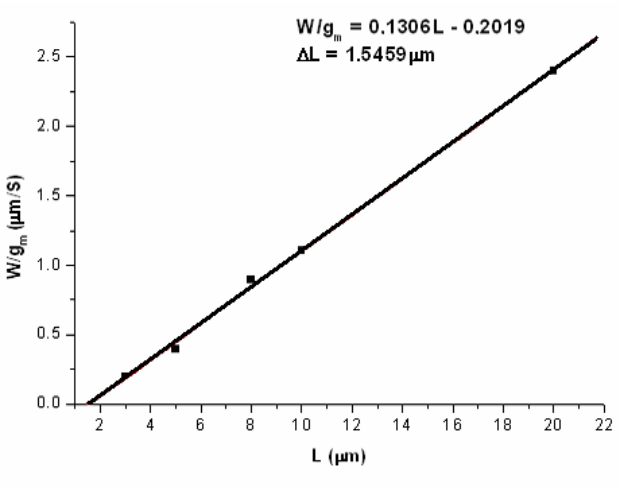

Figure 2. Graphical method to determining ΔL.

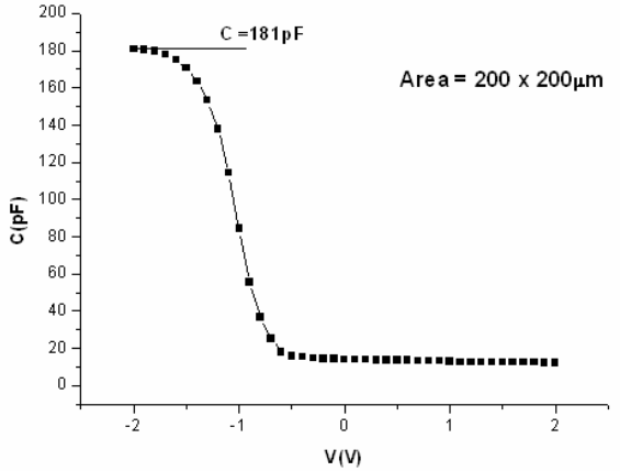

Figure 3. Capacitance curve.

Therefore, the electron mobility was calculated according to equation (4). Table (1) shows the electron mobility of three transistor with different channel length..

$$g_m = \frac{W.C_{OX}.V_{DS}}{L}.\mu_N \Leftrightarrow \mu_N = \frac{L}{W.C_{OX}.V_{DS}} g_m \quad (4)$$

Table 1. Electron mobility of nMOS transistors.

L (μm)	μ_N (cm^2/Vs)
10	169.08
5	137.48
3	172.09

3. COMPUTER SIMULATION

In this work, the computer simulations of transistors and capacitors were performed by the software ADS. The results were obtained from the measures of Grado's and Barros' capacitors in the laboratories of CCS.

3.1. Transistor simulation

Figures 4 and 5 show the necessary layouts to implement the computer simulation by ADS.

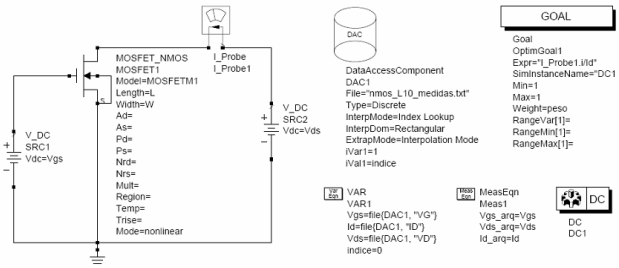

Figure 4. Primary circuit.

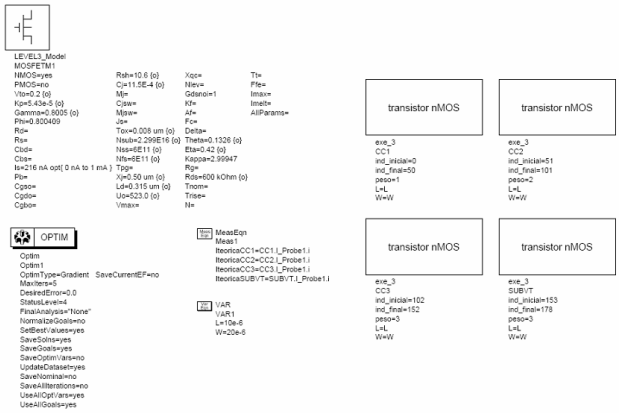

Figure 5. Secondary circuit.

It can be seen in Figure 4 the basic structure of a circuit with a nMOS transistor. Essentially, the results of the measures obtained in the laboratories were organized in a input file and loaded in DAC (Data Acess) component. With these data available the program performs the simulation by comparing the values of the measures with the theorical model of the component, so it returns the parameters of the component as well as the resultant error. Through iterative simulations these values are updated and when the desired error is reached, the user has a good aproximation of these parameters. There are several disponible MOS transistors models in ADS but we have chosen the SPICE Level 3, due its simplicity as well as it contains the main parameters of nMOS transistors [3].

In Figure 5 we can see the SPICE model icon and other necessary components. Each retangular icon (transistor nMOS) contains the whole circuit of the Figure 4, and each one is responsible to run a specific part of the input file. Therefore they were displayed in hierarquic levels, so some circuits had priority in simulation than others. Also it is possible to setup the mathematical method for determining the parametrs. In icon OPTIM (Optimization) there are several available methods, such as Random, Gradient or Quasi-Newton.

Figure 6 shows the curves of a nMOS transistors with L = 5μm. For I_D x V_{DS} curve, the voltage V_{GS} were raised from 0V to 3V with a step of 0.5V, where V_{DS} is the drain/source voltage. In simulation the measured curve remained constant, as the simulated curve might vary according to user's adjust, so a good evaluation of parameters happened when both curves became coincident.

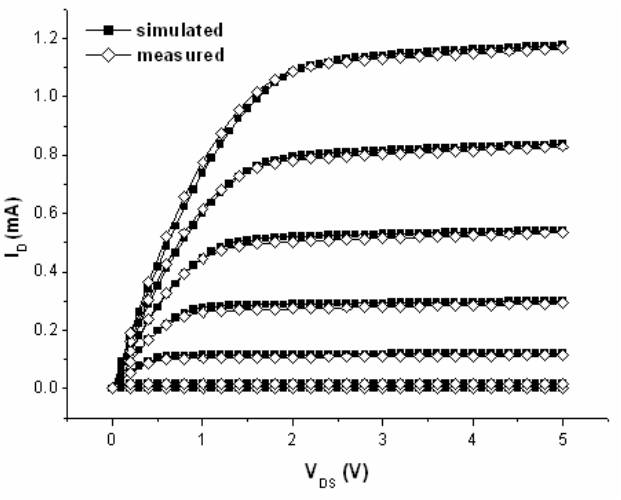

Figure 6. I_D x V_{DS} curve.

3.2. Capacitor simulation

The simulation of the Barros' capacitor was done according to structure in Figure 7. In laboratory, the capacitance analyzer equipment was responsible to provide a constant frequency of 1MHz while the gate voltage (V_{GS}) was varied from –2.5 to 0.5V. For simulate these identical conditions, we used a frequency source that is represented by a resistance of 50Ω. The capacitance block DC_Block acts as a DC filter, as long as it has a hypothetical infinitive capacitance. On the other hand the block DC_Feed filters all unwanted AC signal from the font below, considering its infinitive inductance [3].

We have observed that the SPICE could not properly provide sufficient parameters for MOS capacitors, so for this task we have used the BSIM Level 3.

Figure 8 shows the curves simulated in ADS and measured in laboratory. It can be seen a good approach in accumulation region and in inversion region there was a slight difference between both curves.

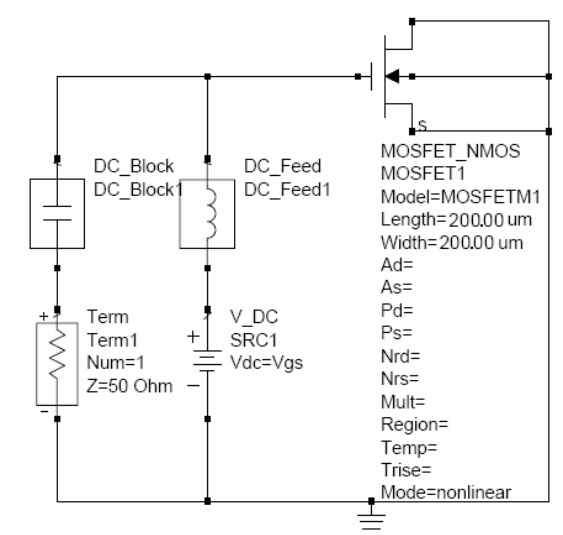

Figure 7. Detail of the circuit for capacitance simulation.

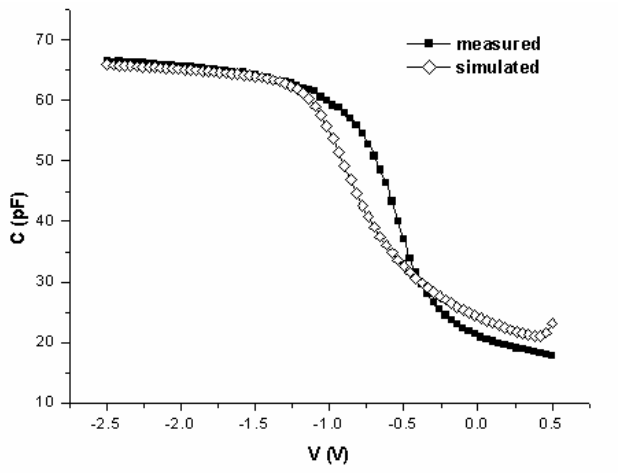

Figure 8. Capacitance curves.

4. CONCLUSION

Several parameter extractions by mathematical and computer methods were proposed and evaluated in this study. There is a high potential of studies in this area, and their applications are very promising in electronic industry. The program ADS provided a powerful tool in simulation and optimization processes. Also we have observed that each model, such as SPICE and BSIM, was suitable according to its application. For the transistor optimization, the SPICE model was sufficient to provide us all the basic parameters and we had to use the BSIM model to capacitor simulation.

5. REFERENCES

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[2] J. A. Martino, M. A. Pavanello, P. B. Verdonck, "Caracterização Elétrica de Tecnologia e Dispositivos MOS", Pioneira Thomson Learning, 2003.

[3] ADS 2006 Guide, Agilent Technologies.