MULTIPLES THRESHOLD VOLTAGES IN TRAPEZOIDAL CHANNEL MUGFETS

Maria Glória Caño de Andrade and João Antonio Martino

LSI/PSI/USP, University of Sao Paulo
Av. Prof. Luciano Gualberto, trav. 3 n. 158, 05508-900, Sao Paulo, Brazil

ABSTRACT

The impact of the sidewall inclination angle on the threshold voltages has been studied through three-dimensional numerical simulation in double-gate, triple-gate and quadruple-gate SOI transistors for a large range of channel doping concentrations for the first time. The results indicated that in MuGFETs transistors it is possible to observe more than one threshold voltages. In double-gate and quadruple-gate transistors, one or two threshold voltages can be observed, depending on the channel doping concentration. However, in triple-gate it is possible to observe up to three threshold voltages depending on the sidewall inclination angle and channel doping concentration due to the corner effect and surfaces inversions.

1. INTRODUCTION

Multiple-gate field-effect transistors are devices with a gate folded on different sides of the channel region that represent promising alternative architectures for future CMOS technology generations. Fig. 1 shows the double and triple SOI transistors and fig. 2 shows the quadruple-gate devices and its correspondent cross-sections channel regions.

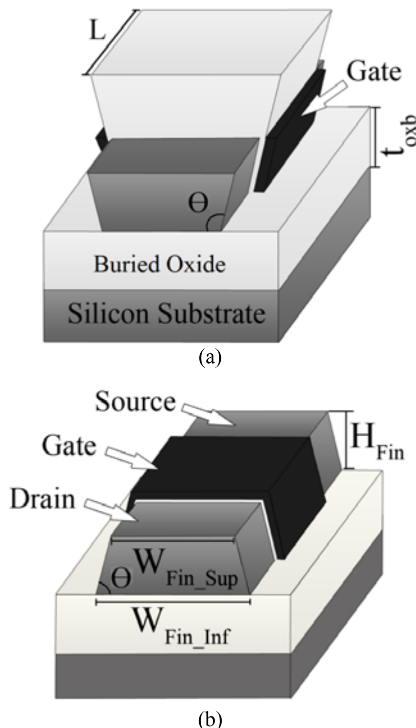


Figure 1. MuGFETs with sidewall inclination angle: double-gate with Θ > 90º (a); triple-gate with Θ < 90º (b).

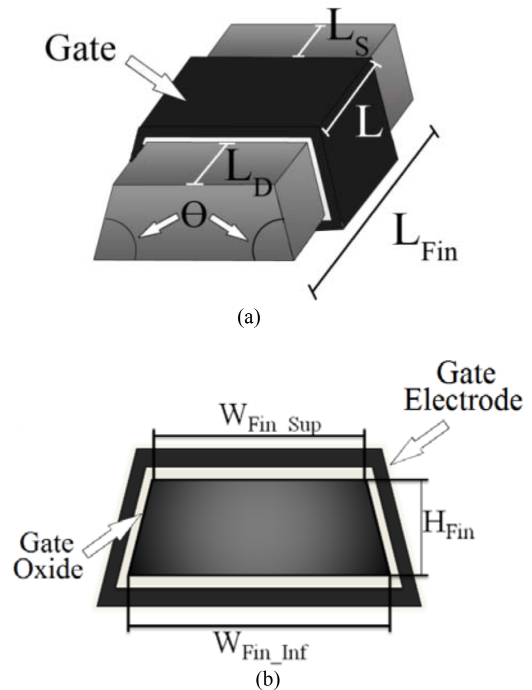


Figure 2. Quadruple-gate SOI MuGFETs with sidewall inclination angle Θ < 90º (a) and its correspondent cross-section view (b).

MuGFETs present superior control of short channel effects and near-ideal subthreshold slope resulting from electrostatic coupling between the channel and the surrounding gate electrode that is enhanced when increasing the number of gates from two to four. On the other hands these architectures present corner effects that depend on the channel doping.

The influence of trapezoidal channel on the FinFETs [1 – 3] and the multiple threshold voltages in rectangular MuGFETs [4, 5] has been published by the literature. In this paper, it is reported how the sidewall inclination angle and channel doping concentration can affect the threshold voltage in MuGFETs devices.

Due to the top and bottom corners, and the conditions the top, bottom and sidewalls surfaces of the fins, the MuGFETs can present more than one threshold voltages. The double, triple and quadruple-gate SOI transistors are studied in this paper as a function of a large range of the channel doping concentration for the first time.

2. DEVICES CHARACTERISTICS AND SIMULATION DETAILS

The simulated structures present a gate oxide thickness of 2 nm, buried oxide thickness (t_{oxb}) of 145 nm, drain and source length (L_D, L_S) of 100 nm each. The fin height (H_{Fin}) is 60 nm, the width of fin W_{Fin_Inf} is equal to 120 nm and W_{Fin_Sup} range 50.6 to 190 nm. The channel length (L) is 1 μm in order to avoid any of short channel effect. The sidewall inclination angle changes from 60 to 120 degrees and gate material is TiN. The silicon doping concentrations for drain and source are $N_D = 1 \times 10^{20}$ cm^{-3}, the channel doping concentration ranging from $N_A = 1 \times 10^{15}$ cm^{-3} to $N_A = 5 \times 10^{19}$ cm^{-3}. The interface charge densities of 3×10^{10} cm^{-2} and the applied voltage to the drain of $V_D = 100$ mV is used. The 3-D numerical simulator used is Atlas of Silvaco [6].

In this work the threshold voltage is extracted by the maximum transconductance charge method [7, 8], because it is appropriate to obtain easily more than one threshold voltage where each transconductance derivative peak is related to one threshold voltage.

3. SIDEWALL INCLINATION ANGLE DEPENDENCE

3.1. Double-gate transistors

In double-gate devices it is possible to note the transition from one to two threshold voltages and the increase of threshold voltage with increased channel doping concentration (fig. 3).

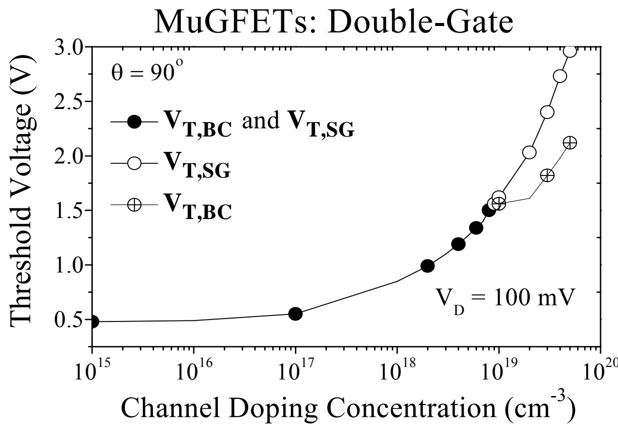


Figure 3. Threshold voltage versus channel doping concentration for double-gate devices with W_{Fin_Inf} and $W_{Fin_Sup} = 120$ nm, $H_{Fin} = 60$ nm and L = 1 μm [4].

The second derivative of the drain current versus gate voltage is shown in figure 4. It is possible to observe two threshold voltages i.e., two peaks of the I_D x V_G second derivative curve in figure 4a for higher N_A (> 10^{19} cm^{-3}).

The lower V_T (the first peak) is related to the inversion of bottom corners ($V_{T,BC}$ is the bottom corners threshold voltage) due to the substrate and sidewall coupling (sum of electric field vectors of the substrate and sidewall gate).

The higher V_T (the second peak) corresponds to the inversion of the sidewalls surfaces controlled by the sidewalls gates ($V_{T,SG}$ is the sidewalls surfaces threshold voltage) [4, 5].

The I_D x V_G second derivative curve (fig. 4b) exhibits a single peak for lower N_A. This threshold voltage is due to bottom corners and sidewalls surfaces inversion at the same time that $V_{T,BC} \cong V_{T,SG}$ [4, 5].

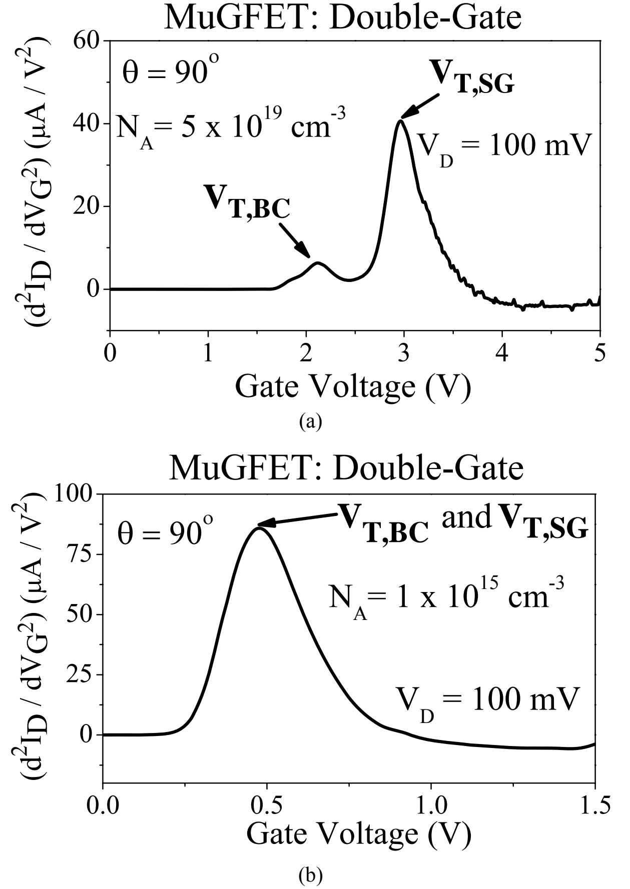
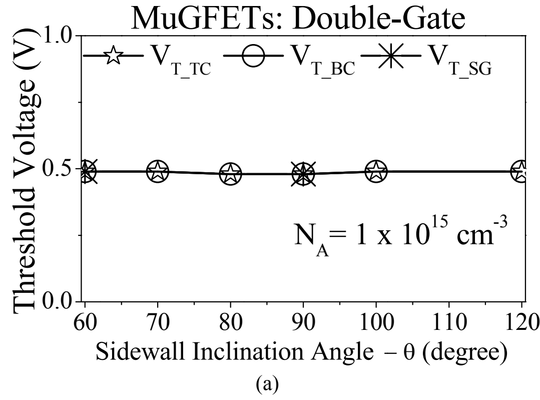


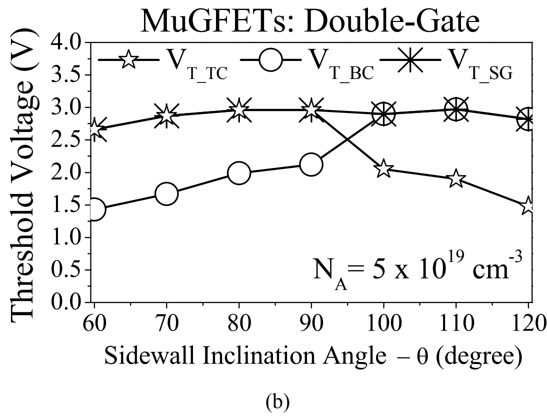
Figure 4. Second derivative of the drain current versus gate voltage for double-gate devices with: $N_A = 5 \times 10^{19}$ cm^{-3} (a);$N_A = 1 \times 10^{15}$ cm^{-3} (b) [4].

Figure 5 shows the influence of sidewall inclination angle (θ) on the threshold voltage behavior for double-gate transistor. For lower N_A (fig. 5a), in all sidewall inclination angle, the inversion surfaces occurs simultaneously, then it is possible to observed only one threshold voltage, $V_{T,TC} \cong V_{T,BC} \cong V_{T,SG}$.

For higher N_A (fig. 5b) it is possible to observe more than one threshold voltages. Devices with sidewall inclination angle is smaller than 90° the higher V_T corresponds to the inversion of the top and sidewalls surfaces ($V_{T,TC} \cong V_{T,SG}$) and the lower is related to the inversion of bottom corners ($V_{T,BC}$). However for sidewall inclination angle is larger than 100° the higher V_T is the inversion of the bottom and sidewalls surfaces ($V_{T,BC} \cong V_{T,SG}$) and the lower threshold voltage is due to the inversion of top corners ($V_{T,TC}$) due to the increase of electric field near the top corner as can be observed in figure 6.

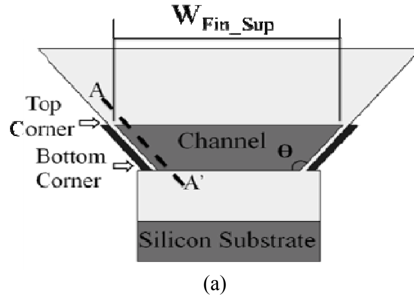


(a)

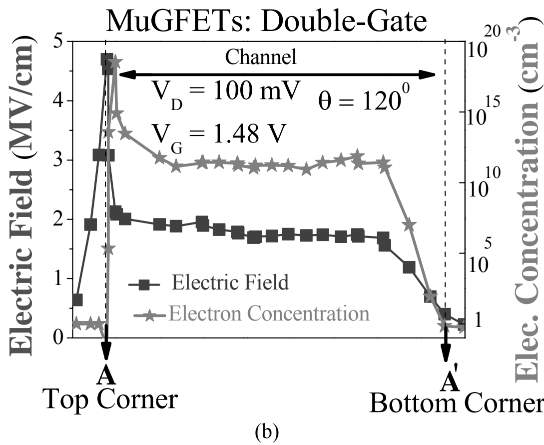


(b)

Figure 5. Threshold voltage versus sidewall inclination angle for double-gate transistors with V_D = 100 mV: (a) N_A = 1 x 10^{15} cm^{-3}; (b) N_A =5 x 10^{19} cm^{-3}.



(a)



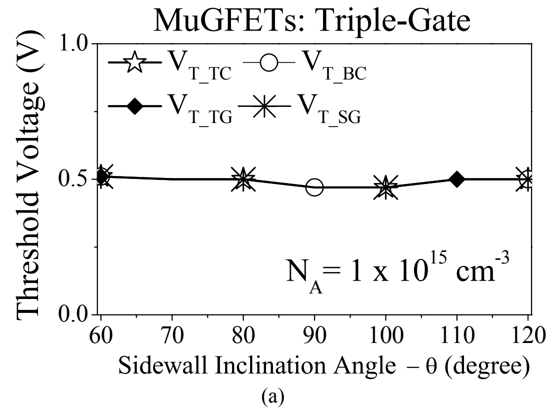
(b)

Figure 6. Cross-section view of the double-gate transistors with sidewall inclination angle (θ = 120º) indicating the line A–A' (a); electric field and electron concentration curves along the line A–A' for lower threshold voltages where $V_{T,BC}$ = V_G = 1.48 V (b).

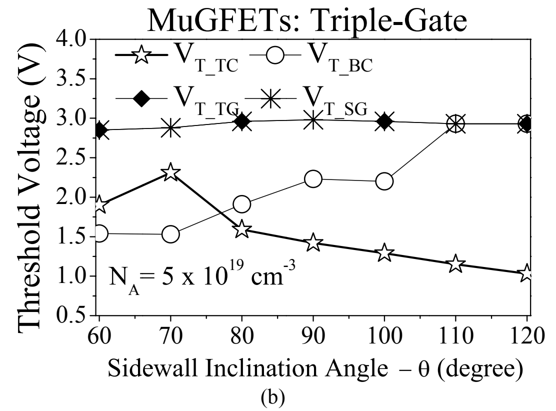
3.2. Triple-gate transistors

Figure 7 presents the same curve showed in figure 5 but for triple-gate transistor. For lower N_A (fig. 7a) as in the double-gate devices it is possible to observe for all sidewall inclination angle only one threshold voltage, where $V_{T,TC} \cong V_{T,BC} \cong V_{T,TG} \cong V_{T,SG}$.

Devices with higher N_A (fig. 7b) present up to three threshold voltages. For sidewall inclination angle is smaller than 77° (fig. 8), the lower V_T is due to the inversion of bottom corners ($V_{T,BC}$), the other V_T is the inversion of the top corners ($V_{T,TC}$) and the higher V_T corresponds to the inversion of the top and sidewalls surfaces ($V_{T,TG} \cong V_{T,SG}$).



(a)



(b)

Figure 7. Threshold voltage versus sidewall inclination angle for triple-gate transistors with V_D = 100 mV: (a) N_A = 1 x 10^{15} cm^{-3}; (b) N_A =5 x 10^{19} cm^{-3}.

For sidewall inclination angle from 77° to 110° the lower V_T is due to the inversion of top corners ($V_{T,TC}$) and the higher one corresponds to the inversion of the bottom corners ($V_{T,BC}$), this is because the bottom curvature radius begins to increase so that the bottom corner effect is decreased [9].

The higher V_T corresponds to the inversion of the top and sidewalls surfaces ($V_{T,TG} \cong V_{T,SG}$). When the sidewall inclination angle is larger than 110° there are two threshold voltages, $V_{T,TC}$ and the $V_{T,BC} \cong V_{T,TG} \cong V_{T,SG}$ (inversion of the bottom corners, top and sidewalls surfaces at the same time). For this sidewall inclination angle, the bottom corner effect is not significant because the bottom curvature radius is larger.

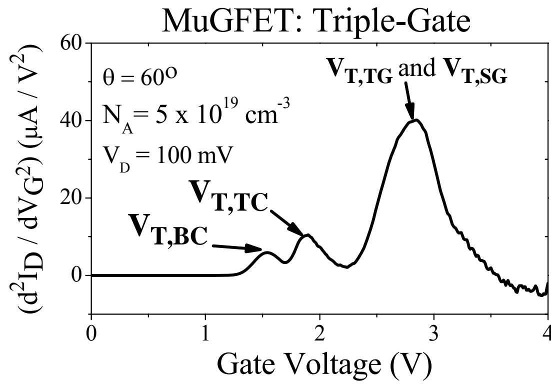


Figure 8. Second Derivative of the drain current ($d^2 I_D/dV_G^2$) versus gate voltage for triple-gate transistor sidewall inclination angle θ = 60º.

3.3. Quadruple-gate transistors

The influence of sidewall inclination angle on the threshold voltage behavior for quadruple-gate transistor is presented in figure 9.

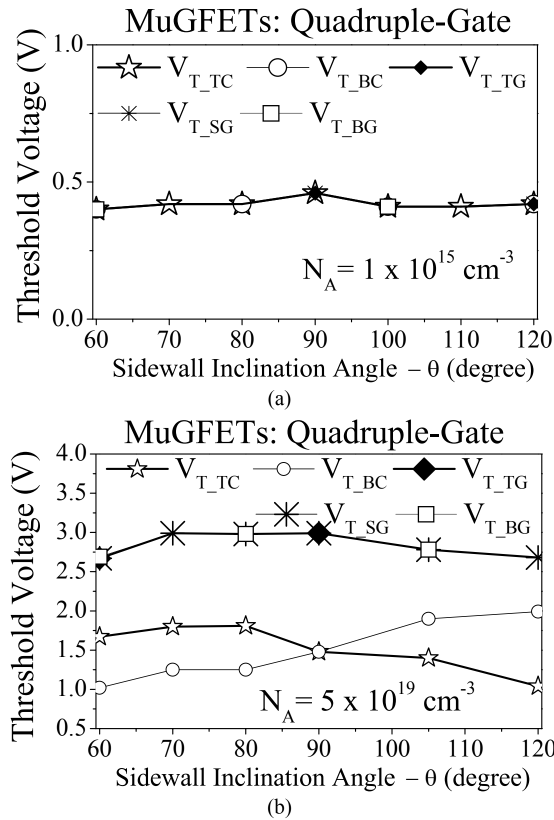


Figure 9. Threshold voltage (V_T) versus sidewall inclination angle (θ) quadruple-gate transistors with W_{Fin_Inf} = 120 nm, H_{Fin} = 60 nm, L = 1 µm and V_D =100 mV: (a) $N_A = 1 \times 10^{15}$ cm^{-3}; (b) $N_A = 5 \times 10^{19}$ cm^{-3}.

For higher N_A (fig. 9b) with sidewall inclination angle is smaller than 90° it is possible to observe three threshold voltages, where corresponds to the first one (the lower) is the $V_{T,BC}$, the second one is $V_{T,TC}$ and the higher threshold voltage is inversion of the top, bottom an sidewalls surfaces ($V_{T,SG} \cong V_{T,TG} \cong V_{T,BG}$).

When the sidewall inclination angle is larger than 90°, firstly occurs the inversion of the top corner due to the top curvature radius is smaller than the bottom one, consequently the corner effect will be larger. Although with lower N_A (fig. 9a) all inversion occurs at the same time and $V_{T,TC} \cong V_{T,BC} \cong V_{T,TG} \cong V_{T,SG} \cong V_{T,BG}$.

4. CONCLUSION

The simulations results of this paper indicated that for double-gate devices with higher channel doping concentrations when the sidewall inclination angle is increased the bottom curvature radius is also increased as a consequence the bottom corner effect is reduced. However, it was also observed that the top corner effect appears due to the high electric field near to the top.

In triple-gate and quadruple-gate transistors for small sidewalls inclinations angle, the lower V_T is due to the inversion of the bottom corner ($V_{T,BC}$). However, if the Θ angle increases, the lower threshold voltage becomes $V_{T,TC}$ thanks to the decrement of top corners angle. For lower channel doping concentrations independent of sidewall inclination angle it is possible to observe only one threshold voltage for all the MuGFETs studied in this work.

5. ACKNOWLEDGMENTS

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6. REFERENCES

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