

THE CORNER EFFECT INFLUENCE ON DRAIN CURRENT IN LOW-DOPPED ROUNDED CORNERS TRIPLE-GATE DEVICES

Rodrigo Prior Bechelli^a, and R. Giacomini^{a,b}

^a Department of Electrical Engineering, FEI, S. B. do Campo, SP, Brazil.

^b LSI/PSI/EPUSP, University of São Paulo, São Paulo, SP, Brazil.

ABSTRACT

For low-doped rounded-corner devices, the second peak on the second derivative of drain current versus gate voltage curve may not appear and the threshold voltage can be characterized by a single peak, using the maximum transconductance change method. The second peak suppression might induce to the irrelevance of the corner effects for such devices. In this work we evaluate, through three-dimensional numeric simulation, the influence of corner effects on carrier distributions and on the drain current for devices where the second peak does not appear. We conclude that the corner effect may still be relevant for some devices and for these transistors it should be considered in modeling and design activities.

1. INTRODUCTION

Industry seeks for new alternative device configurations in order to surpass the classical MOS structure performance, as it gets closer to scale limits. One of these alternatives is to move from planar structures to three-dimensional multiple-gate devices, as a solution to reduce short-channel effects and increment current drive [1]. These new devices brought new concepts and challenges to research. One of them is the existence of corner effects, a higher carrier density that occurs near the corner regions of multiple-gate devices [2] [3]. This effect is caused by the simultaneous influence of two gate planes on these regions what increases the electric potential. Some research was made on how to reduce this effect by controlling the corner curvature radii or reducing the channel doping concentration [4]. The corner effect is usually characterized by a second peak on the second derivative of the drain current as a function of the gate bias. This second peak is suppressed with corner radii increase and with lower doping levels. In this work it is considered that corner effects can occur in lower concentrations and different corner radius, as a result of gradual influence of the higher electrical field over the corner region.

We analyze the corner effect by observing the electron concentration at the device cross-sections and comparing the corner values at the lateral gates to the values at the corners. The use of three-dimensional numeric simulation allows the comparative analysis between devices with different doping levels and corner curvature radii. This paper also studies the drain current behavior for these devices.

2. SIMULATED DEVICES

The triple-gate simulated device is schematically represented in figure 1, and presents buried oxide thickness (t_{BOX}) of 200 nm, gate oxide thickness (t_{OX}) of 3 nm for the three gate planes and interface charge density of $3.0 \times 10^{10} \text{ cm}^{-2}$. Work function of 4.15 eV was adopted for the gate material. The silicon active region was designed as a square ($H=W$) of 50 nm with gate length (L) of 200 nm for all simulations.

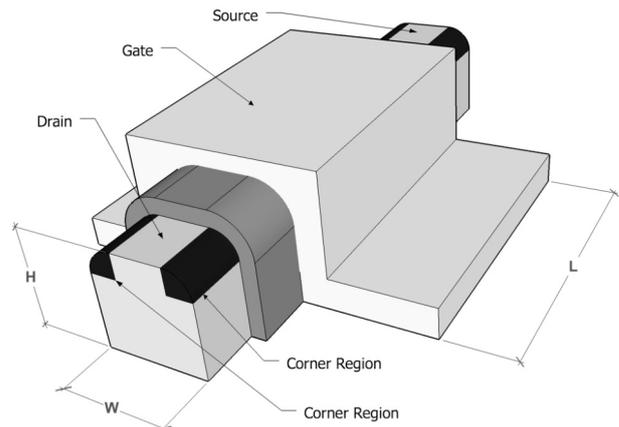


Figure 1: Rounded Corner Triple-gate simulated device, W – fin width, H – fin height and L – channel length.

The work was developed using Silvaco Atlas three-dimensional numeric simulator. The mentioned second peak in the second derivative of $I_{\text{DS}} \times V_{\text{GS}}$ curves occurs in a well-defined characterization parameters: gate doping concentration higher than $3 \times 10^{18} \text{ cm}^{-3}$ and low radii curvature corners. [2] [5] [6]. Four different silicon doping concentrations (N_{a}) were selected: 10^{16} cm^{-3} , 10^{17} cm^{-3} , 10^{18} cm^{-3} and $3 \times 10^{18} \text{ cm}^{-3}$. Three different corner radii were adopted: from typical values of $R = 2.5 \text{ nm}$ and 5 nm to a high value of 12.5 . Sharp corner devices ($R=0$) were also simulated for drain current comparison. Figure 2 shows the second derivative curves obtained. For the higher adopted doping level the second peak can already be observed, for radii smaller than 12.5 nm .

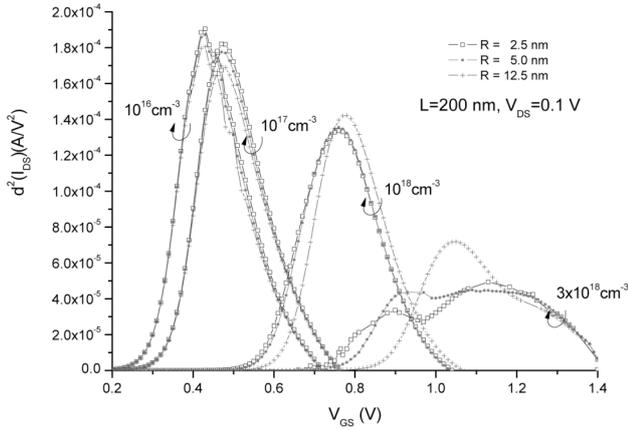


Figure 2 – Second derivative of $I_{DS} \times V_{GS}$ curve, showing the single peak for some devices and the second peak for the devices with higher doping level and smaller radii.

The threshold voltage (V_{TH}) was obtained from the drain current (I_{DS}) versus gate voltage (V_{GS}) curve extrapolation for $V_{DS}=10mV$. See results for rounded corner devices in Table 1. The “extrapolated” V_{TH} was calculated by the interception of tangent and horizontal axis. Impact ionization models were considered even for low drain voltages. Quantum effects were not considered. Table 1 shows V_{TH} for the considered devices. The threshold voltage does not depend on the corner radius.

| Na (cm^{-3}) | H=W (nm) | | |
|---------------------|--------------------|-------------------|----------------------|
| | 5% (R = 2.5 nm) | 10% (R = 5 nm) | 25% (R = 12.5 nm) |
| 1×10^{16} | 0.41 V | 0.42 V | 0.43 V |
| 1×10^{17} | 0.47 V | 0.47 V | 0.47 V |
| 1×10^{18} | 0.76 V | 0.76 V | 0.7 V |
| 3×10^{18} | 1.13 V | 1.07 V | 1.04 V |

3. CHARGE DISTRIBUTION AT THRESHOLD VOLTAGE

A good way to measure the influence of corner region in N-channel devices is verifying the electron concentration and comparing the corner values with other regions like the center of the lateral or upper channels at the Si/SiO₂ interface. In this work, the electron concentration was analyzed at cross sections at the middle of channel length ($L/2$), see figure 3.a.

Each transistor was biased at the respective threshold voltage, using the values of V_{TH} from Table 1. From this cross-section bi-dimensional electron distribution, two different cut lines were adopted, as shows figure 3.b: one horizontal cut from the center of the silicon fin to the Si/SiO₂ interface (cut1) and a diagonal from the center to the upper corner (cut2). Curves of electron concentration versus the distance from the center to the interface Si/SiO₂ were plotted, normalizing the distance from the center to the interface for better comparison.

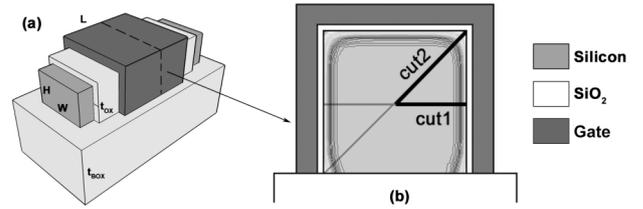
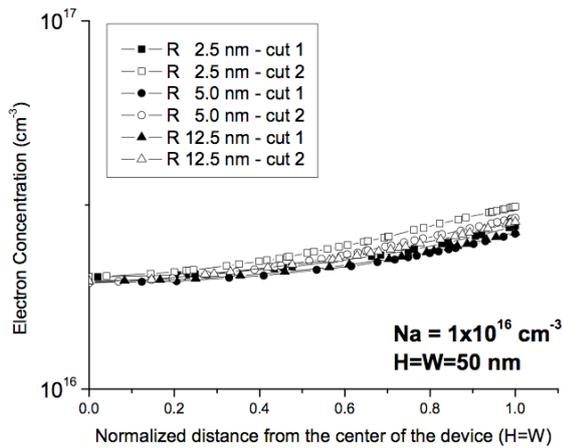


Figure 3: (a) Triple-gate device, t_{OX} - gate oxide thickness, t_{BOX} – buried oxide thickness, W – fin width, H – fin height and L – channel length. (b) Transversal cut at the middle of channel and two cut lines – cut1 and cut2

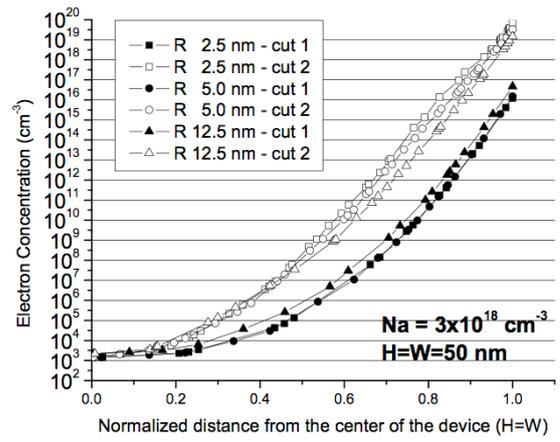
Curves obtained by this process were classified by doping concentrations. As a consequence of the distance normalization, the 0 (zero) value represents the center of the device and 1 (one) is the Si/SiO₂ interface. The corner effect can be observed by comparing the filled-marker (cut1) to the non filled-marker curves (cut2) in figures 4.a through 4.d.

It can be seen that electron concentration is always higher at the corners. The influence of the doping level can be analyzed by comparing Figures 4.a through 4.d. Figure 4.a presents extracted curves from devices with doping concentration of $10^{16}cm^{-3}$. It can be seen that electron concentration curves of cut1 and cut2 are quite near one from another for the three corner radius. As the doping level increases (Figures 4.b, c and d) the distance between the concentration values of cut1 and cut2 also increases, what shows a strong dependence of corner effect on the doping level, as expected. Figure 4.d ($3 \times 10^{18}cm^{-3}$) shows a difference of almost three decades in the electron concentration near the interface Si/SiO₂ for the two cut lines (cut1 and cut2).

The corner radius also influences the corner electron concentration. Comparing cut1 and cut2 electron concentrations in Figures 4.a through 4.d it is possible to identify a slightly different behavior in the corner when radius (R) change from 5% (2,5 nm) to 25% (12.5 nm): small radius have a higher electron concentration if compared to other radius sizes.



(a)

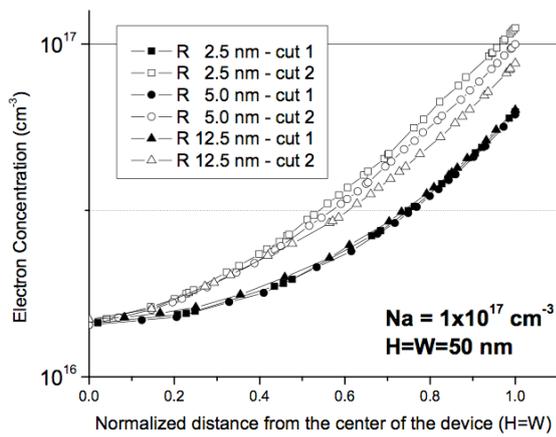


(d)

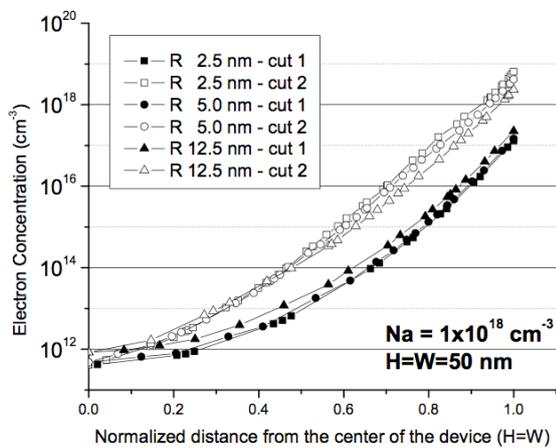
Figure 4: Electron Concentration Curves versus normalized distance from the center.

4. DRAIN CURRENT

The precedent section showed that the charge distribution method of analysis allow the comparison of different geometries and doping concentrations. The corner effects can also be observed on the drain current. In Figure 5 it is possible to identify variations in the of $I_{DS} \times V_{GS}$ curve slopes. As the corner radius increase, the curves present smaller drain currents. Curves from Figure 5 were traced with $V_{DS}=10\text{mV}$ presenting the drain current (I_{DS}) versus gate voltage (V_{GS}) for the simulated transistors.



(b)



(c)

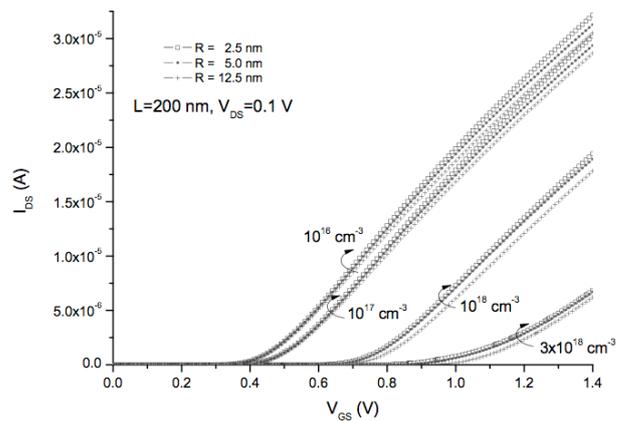


Figure 5: $I_{DS} \times V_{GS}$ Curves: rounded corner transistors.

Figure 6 shows the normalized current I_{DS}/I_{0DS} , where I_{0DS} is the current obtained for sharp corners ($R=0$). The two lower doping levels are almost coincident and have less influence of the corner radius on the drain current. As the doping level is increased, the dependence grows. For all curves the slope decreases as the radius increases, but is always finite, even for very the large radius value of 12.5 nm.

The result of this analysis is described in Figure 6 where it was set a gate voltage (V_{GS}) of 1.4V for all simulated transistors. Different corner radius and different channel doping levels were compared. Drain current decreases as corner radius increases.

The sharp corner transistors ($R=0$ nm) are plotted just as a reference, once these devices are not realistic, because of the silicon oxidation and other gate construction steps of the fabrication process. Some processes include an special step to adjust the corner radius. But Figure 6 shows that even for devices that do not present the second peak, the corner effect on the drain current is considerable. The 10^{16} cm^{-3} and 10^{17} cm^{-3} doped devices present a variation of 5,4% in the drain current, when the corner radius changes from 2.5 to 12.5 nm. The same result occurs for lower doping levels. This value grows to over 9% for the 10^{18} cm^{-3} doping level that still do not present the second peak in the second derivative of the $I_{DS} \times V_{GS}$ curves.

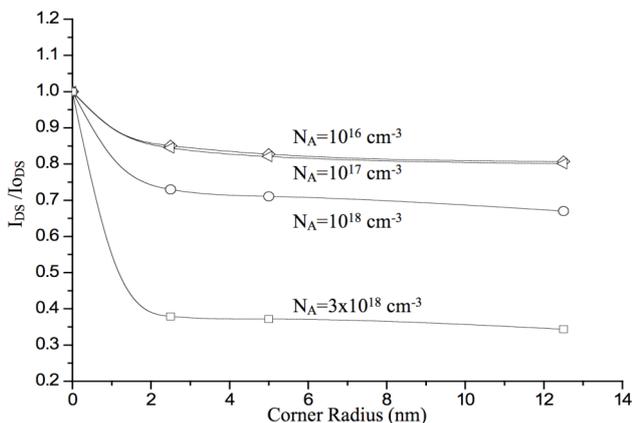


Figure 6: Normalized Drain Current (I_{DS}/ I_{0DS}) versus Corner Radius Curvature (R).

5. CONCLUSION

Drain current and electron concentration were analyzed for rounded-corner triple-gate devices, for doping levels from 10^{16} cm^{-3} to $3 \times 10^{18} \text{ cm}^{-3}$ and corner radii from 0 to 12.5 nm, through three-dimensional numeric simulation. Even for devices where there is not a second peak on the second derivative of the $I_{DS} \times V_{GS}$ curve, the drain current showed to be dependent on the corner radius, what means that the corner effects are still present for such devices. For doping levels lower than 10^{17} cm^{-3} the current changes near 5% when the corner radius changes from 2.5 to 12.5 nm.

6. REFERENCES

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