FIRST AND SECOND ORDER SUBSTRATE BIAS INFLUENCE ON FINFETS

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ABSTRACT

The substrate bias influence on the first and the second order effects and the relationship with the lateral gates coupling are studied in this paper for SOI FinFETs. Simulations for several fin widths were performed to evaluate the threshold voltage susceptibility to the substrate bias and the electric potential profile behavior on the fin. The potential distribution along the fin showed to be dependent on the lateral gates coupling and as a consequence, different behaviors were observed on the threshold voltage in function of substrate bias.

1. INTRODUCTION

The requirements for the continuous evolution of MOS transistors with a good scalability performance may be achieved by multiple-gate SOI MOSFET devices, due to their better control of channel charges [1-2], reducing short channel effects, mainly on narrower fins. One of the most promising and attractive multiple-gate structures being developed is the SOI FinFET, allowing the further downscaling of devices achieving extremely reduced dimensions [3] and channel lengths as short as 10nm [4], also presenting good electric characteristics in analog and digital applications [5], a good frequency response in unitary gain and intrinsic gain [6], following a fabrication process that does not differ significatively of SOI CMOS traditional process [7]. The dual gate SOI FinFET, also known as DELTA, was first developed in 1989 with a thicker gate oxide at the top, followed by the triple gate FinFET which passed through enhancements in the fabrication process, especially on the gate oxidation step, allowing the formation of a thin and uniform gate oxide on the three gate planes, resulting in a superior control of the channel charges. As the fin width gets thinner, the proportion of the drain current that will flow through the lateral walls will increase and can even surpass the drain current quota flowing over the top of the channel, closing to a condition were it start to behave like a dual gate device. FinFET devices often present volume inversion, distributing the minority carriers over the entire fin, and achieving good mobility levels inside the silicon film.

In this work the substrate bias influence on the threshold voltage and the electric potential distribution along the cross-section of the fin are evaluated, confronting simulation results with experimental ones.

2. SIMULATED DEVICES

Simulations were conducted using Silvaco Atlas Three-Dimensional Device Simulator for devices with Fin Width (W_{Fin}) ranging from 20nm to 10µm, fin height (H_{Fin}) of 60nm, gate oxide thickness of 2nm, buried oxide thickness of 145nm, channel length fixed in 1µm and channel doping level of $N_A=1x10^{15}cm^{-3}$.

3. EXPERIMENTAL DEVICES

The measured experimental devices are state-of-the-art FinFETs with n-channel type ($N_A=1x10^{15}cm^{-3}$), fabricated at Interuniversity Microelectronics Center (IMEC), in Belgium, following the process described in reference [8]. As the simulated devices, the fin height is equal to 60nm and the buried oxide thickness is 145nm. The gate oxide was formed by a silicon oxide layer of 1nm followed by the deposition of 2nm of hafnium oxide, resulting on an effective gate oxide thickness of 2nm. The fin effective width ranges from 20nm to 10µm.

4. RESULTS AND DISCUSSIONS

4.1. Threshold Voltage

The method used to extract the threshold voltage from I_{DS} x V_{GS} with the drain biased in 25mV (V_{DS}=25mV) for each fin width and substrate bias was the maximum transconductance change (MTC). In this method the threshold voltage is the gate voltage where d^2I_{DS}/dV_{GS}^2 reaches the maximum value [9].

The simulated front-channel threshold voltage values are presented in Figure 1 as a function of the substrate voltage for W_{Fin} ranging from 20nm to 10µm, and Figure 2 presents experimental threshold voltage values also as a function of the substrate voltage. As the substrate voltage is decreased, an increment on V_{th} is noticed. This increment is larger for wider devices than for narrower ones once the channel becomes more exposed to the substrate bias due to the gradual decoupling of lateral gates. Actually, as the back interface regions near the lateral gates belong simultaneously to the front and back interfaces, they do not accumulate when the front gate is biased at the threshold voltage. So, in FinFETs the accumulation at the back interface is always partial. For narrow fins, the accumulation at the back interface is much lower, even for high negative voltages applied to the substrate, both in simulations and measurements. For fin width values as small as 20nm the lateral gates coupling is so high that the threshold voltage almost does not suffer any variation with the substrate bias changes. The measured results presenting this behavior are shown on the top right corner of Figure 2. It is also notable the reduction of V_{th} with the reduction of channel length, due to short channel effects. Recent studies demonstrated that for extreme negative substrate biases, around -80V and -100V, the electric field from the substrate becomes high enough to become dominant again, overcoming the lateral gates coupling [10]. Comparing both graphs it is possible to observe the agreement of the tendency on the threshold voltage values for devices with wider and also narrower W_{Fin}.

For positive substrate bias there is an abrupt elevation of the threshold voltage on devices where the ratio W_{Fin}/L is high (the fin width is much larger than the channel length), a tendency that

agrees with the study [11] by Akarvardar *et al*. This agreement between simulation and experimental data attests the validity of the simulations for the first order effects on I_{DS} and V_{th}, necessary to obtain accurate parameters to characterize the devices.

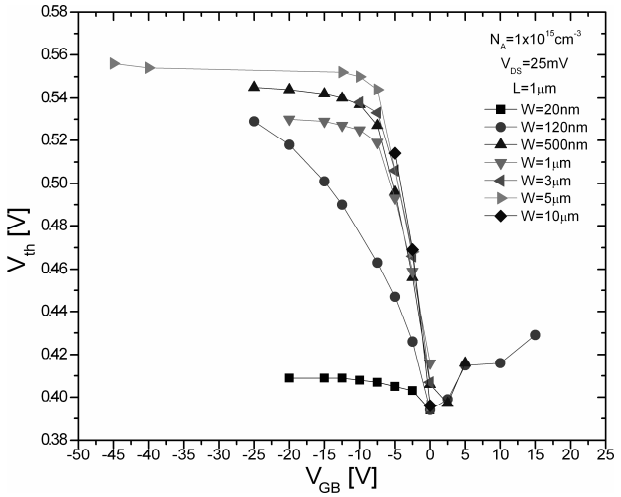

Figure 1. Simulated threshold voltage values as a function of substrate voltage for FinFETs with parallel sidewalls.

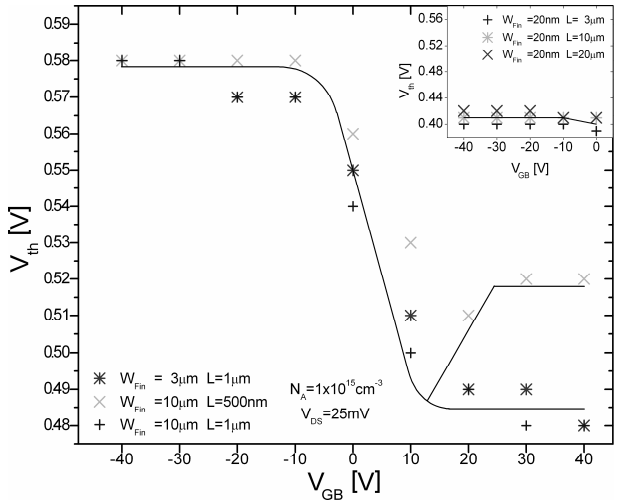

Figure 2. Experimental threshold voltage values as a function of substrate voltage for FinFETs. V_{th} values for very thin fin widths are presented at the top right corner.

4.2. Electric Potential Fin Profile

The effect of the top gate is well known and its influence is dominant in devices with wide fins. For such devices the threshold voltage may be described by the planar model [12], discussed in [11] indicating that the threshold voltage is independent of the lateral gates coupling for fin widths larger than 500nm when are evaluated only the first order effects through V_{th} x V_{GB}.

In order to quantify the lateral gates influence on the second order effects on the analyzed FinFETs, several simulations were performed for dual gate devices to determine W_{Fin} from which the devices can be considered as a planar one. The potential profile perpendicular to the gate planes at half fin height (h=30nm) was extracted for four different fin widths: 120nm, 500nm, 1μm and 3μm and it is presented in Figure 3. The potential at 0V is the reference and corresponds to the neutral region. As the sidewall gates get distant, the potential distributed along the fin decreases until it reaches 0V, where the depletion ends.

From the results obtained through simulations in a double-gate device it is possible to observe the depletion zones extending from the Si-SiO_2 interfaces near the gates to the maximum depletion width. The maximum depletion width ($x_{d.max}$) is classically defined by equation (1), which returns the value of $x_{d.max}$=833nm for the analyzed technology. Thereby, for devices in our configuration with W_{Fin} inferior to 1.67μm ($W_{Fin} < 2 \cdot x_{d.max}$) the interaction between the depletion zones caused by both gates can no longer be neglected, due to the strong coupling between them [7].

In Figure 3, for devices with W bellow 1.67μm (i.e. devices with W equal to 120nm, 500nm and 1μm) there is no plateau between the two gates indicating a fully depleted device, plateau that is present on the device with W=3μm at the potential near 0V, indicating a partially depleted fin.

$$x_{d.max} = \sqrt{\frac{4 \cdot \varepsilon_{Si} \cdot \Phi_F}{q \cdot N_A}} \qquad (1)$$

where: $$\Phi_F = \frac{k \cdot T}{q} \cdot \ln\left(\frac{N_A}{n_i}\right)$$

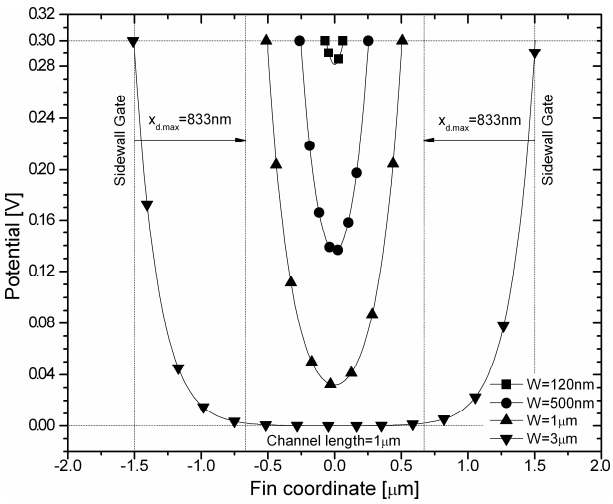

Figure 3 - Potential profile for fins with parallel sidewalls.

The impact of the lateral gates influence on triple-gate FinFETs structures with L=1μm and V_{DS}=25mV for W=3μm and W=10μm was evaluated through the experimental measurements as presented in Figures 4 (a) and (b). From these curves both the first and the second order effects can be identified.

When the focus is the g_m group of curves with V_{GB} varying from 0V to -40V for V_{GF} smaller than 0.875V, it is possible to notice that the g_m shift occurs due to the reaction of V_{th} to the V_{GB} bias following the Lim & Fossum model. When the focus on the curves is given after V_{GF}=0.875V it is possible to observe the GIFBE [13] which is a second order effect dependent of substrate bias. This effect is characterized by the appearance of

the anomalous elevation on the transconductance curves, also referenced as the transconductance second peak, which is highly sensitive to the back interface condition.

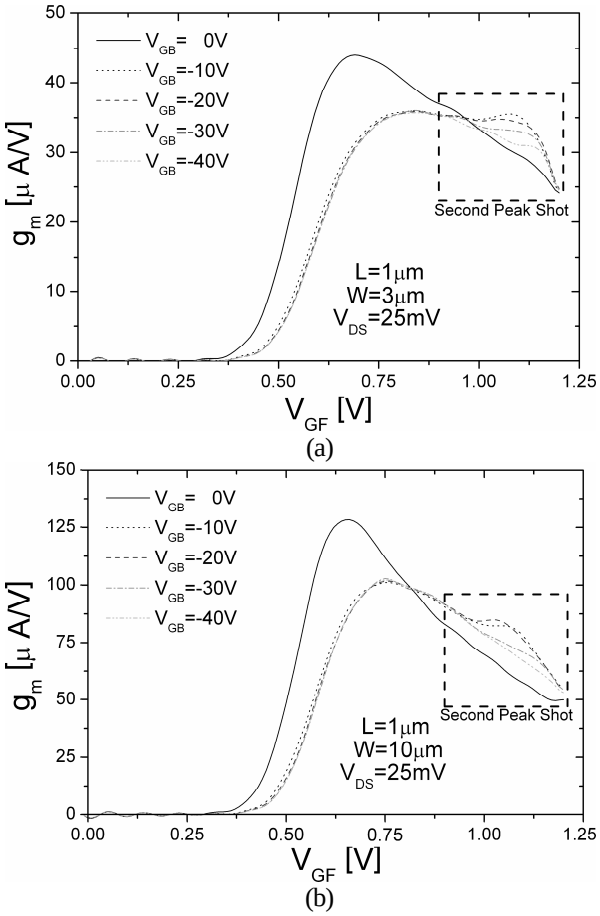

Figure 4 - Measured transconductance curves (g_m) as a function of the bias applied to the gate (V_{GF}) for different substrate voltages (V_{GB})
(a) Fin width equal to 3μm (b) Fin width equal to 10μm

The transconductance second peak shot occurs for different V_{GF} voltages when W=3μm but happens for the same V_{GF}=0.95V value when W=10μm due to the strong dependence with the back accumulation. As showed before, on Figure 3, for dual-gate devices with W=3μm, the accumulation takes place in a small part of the silicon fin at the neutral region at the center of the fin where the lateral gates have no influence on the fin charges, but for W=10μm the accumulation volume is proportionally much bigger than the depletion zones and the back interface is easily accumulated, meaning that even when the depletion coming from the lateral gates does not interact among themselves, if the depletion volumes were proportionally high, their influence on the second order effects can not be neglected.

For transistors with W=3μm, despite the fact that the drain current flows predominantly by the top of the fin since it is much wider than high, the depletion region generated by the lateral gates invades more than the half of the fin width. Thus, the second order effects, as the variation of the potential at the second interface, are much more dependent of this depletion, causing the GIFBE shot for different V_{GF} voltages. For the transistor with W=10μm, the depletion control of almost the entire fin is due to the top gate and the substrate, then for this W_{Fin} the FinFET can be considered as a planar device, even when the second order effects are taken into account.

5. CONCLUSIONS

The data concerning the influence of substrate bias on the threshold voltage and on transconductance second peak for various W_{Fin} on SOI FinFETs were analyzed through experimental and simulation results with the first and the second order effects being considerated. For devices with narrow fins the variation of the potential by the substrate influence is diminished due to the reduction of the accumulation layer near the back interface. Differently from what is found in the literature, stating that if the majority of the drain current flows by the top of the fin and that the dependence of V_{th} with V_{GB} in this case is described by the Lim & Fossum model, it was verified that when the second order effects are taken into account it is necessary to analyze who is responsible for the control of the depletions and how proportionally significant they are on the fin.

On devices much larger than twice the maximum depletion width ($W_{Fin} >> 2 \cdot x_{d.\max}$) the influence caused by the depletion coming from the lateral gates can be neglected, although on devices larger than twice the maximum depletion width, but with a proportionally high penetration of the depletions from the lateral gates into the fin should not be ignored, because of the second order effects, as was seen in the case where W=3μm for the studied technology.

6. ACKNOWLEDGMENTS

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