LAYOUT DESIGN OF CMOS INVERTERS WITH CIRCULAR AND CONVENTIONAL GATE MOSFETs BY USING IC STATION OF MENTOR

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ABSTRACT

This paper describes how to implement the circular and conventional gate CMOS inverters with minimum dimensions by using IC Station of Mentor Graphics. Besides that, it is performed a die area comparative study between these two CMOS inverters, implemented with circular gate and rectangular (conventional) SOI MOSFETs. The technology used to implement these layouts is MOSIS with 0.50 µm, with lambda of 0.35 µm (MEP/MOSIS). Since the circular gate MOSFETs need a smaller area to be implemented, it is interesting to study them and compare their layout with the conventional MOSFETs, in order to use the transistors in analog circuits.

1. INTRODUCTION

The random error effects of the fabrication processes and devices layouts have an important influence in the electrical performance of digital and analog integrated circuits (1, 2), mainly when the matching is necessary, such as operational amplifiers and analog/digital converters. Regarding planar transistors, one alternative is to use the circular MOSFET in order to produce better performance and a smaller die area as compared to the rectangular counterpart (3), as is displayed in Figure 1.

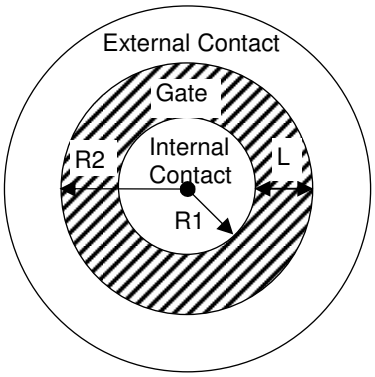

Figure 1: Example of Circular Gate SOI MOSFET (CGT) layout (4).

In Figure 1, L is the channel length (=R2 – R1), and R1 and R2 are internal and external radius of the channel.

The CGT geometric factor (f_g) is given by the Equation [1], where W is the channel width (4).

$$\left(\frac{W}{L}\right)_{Rectangular} = f_g = \left[\frac{2\pi}{\ln\left(R2/R1\right)}\right]_{Circular} \quad [1]$$

The objective of this paper is to implement two CMOS inverters layouts by using circular and conventional MOSFETs and compare the wasted die area of these circuits regarding the MOSIS with 0.50 µm design rules with lambda (λ) of 0.35 µm.

2. CIRCULAR INVERSOR

The CMOS inverters layouts are implemented with two pMOSFETs in parallel, connected in series with one nMOSFET, in order to compensate the mobility difference between holes and electrons and produce a f_g equal to 1, regarding the electron mobility is equal to twice the hole mobility.

The technique to implement CGT with minimum dimensions, first of all, is to implement the internal region (active contact and metal1). After that, we have to implement the circular gate region (polysilicon) and finally the external regions (external contacts and doping area). This device is asymmetric in relation as drain and source regions. Figure 2 presents the SOI MOSFET internal region layout, using the circular gate geometry.

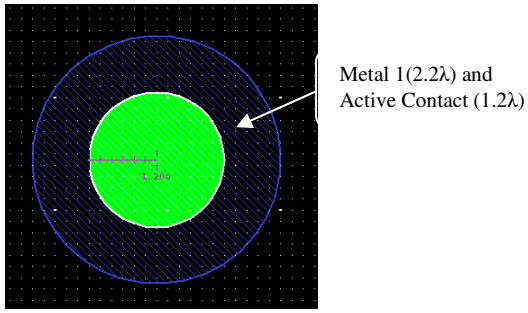

Figure 2: Active contact (internal circle), covered with metal 1 (external circle).

The active contact radius of internal region was calculated by using the same square active contact area of conventional MOSFET. The MOSIS design rules were used to calculate the active contact radius and distance between the active contact and metal1 layers. According to the MOSIS design rules, the minimum active contact radius, which could be implemented, is 1.2λ. The minimum pMOSFET radius is the sum of the radius of the internal contact (3.2λ), with length of the poly silicon ring and a security distance (3λ), with the diameter of a external contact (6.4λ) and the P plus ring (2λ), resulting a value of 14.6λ. The Figure 3 presents the circular pMOSFET layout with length of 2λ, which is the minimum dimension supported for this technology. The layers used to implement this structure are Metal 1, Metal 2, Metal 3, Poly, Active Contact, Active and P Plus Select.

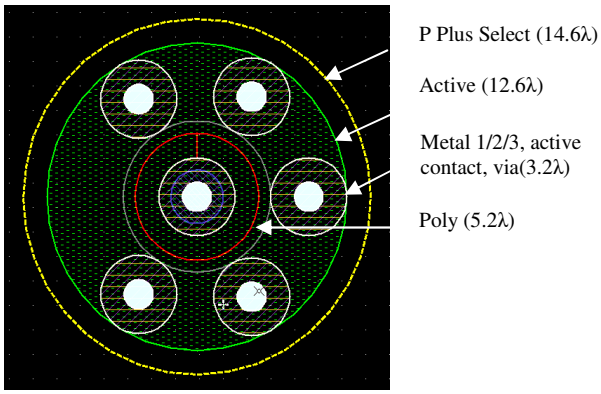

Figure 3: A circular pMOSFET, using the MOSIS rules. Inside the parentheses is displayed the value of the radius of the structure.

After implementing the pMOSFET, a new active region was created, in order to implement a N Plus region and obtain the substrate contact. This area has two active contacts, covered with layers of Metal 1, Metal 2 and Metal 3, whose total diameter is given by 6.4λ. The MOSIS design rules request a distance between two Metal 3 layers equal to 3λ. Following those rules, the distance between the edges of the new active region is 15.8λ. This distance is the sum of the diameter of the two contacts (6.4λ for each contact), plus the minimum distance between the layer Metal 3. The layers used to implement this region are Metal 1, Metal 2, Metal 3, Active Contact, Via, Active and N Plus Select.

Figure 4 presents the pMOSFET with the new active region.

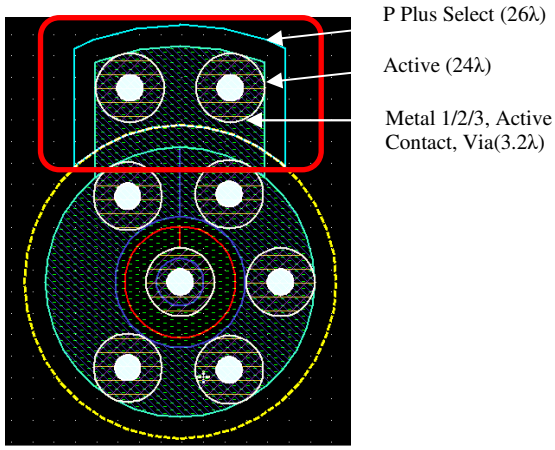

Figure 4: Circular gate pMOSFET with its two substrate contacts. Inside the parentheses is displayed the value of the radius of the structure.

After that, a new circular pMOSFET was created and connected in parallel with the first transistor by using metal 1 and metal 2. The pMOSFETs were connected to each other, using the internal drain configuration by using metal 2 layer and the external drains were connected in parallel with the N Plus regions, by using the metal 1 layer.

Additionally, circular gate nMOSFET was connected in series with the two circular pMOSFETs. This nMOSFET can be implemented, by coping the pMOSFET designed above and changing the doping areas. The area, which was N PLUS, should be edited to become P PLUS and the area, which was P PLUS, now, is N PLUS. The nMOSFET uses the same configuration of internal drain, as the pMOSFETs.

Finally, the ports “IN”, “OUT”, “VDD” and “VSS”, were connected to the PADs, using the Metal 3 layer. Figure 5 presents the final CMOS inverter layout without the PADs.

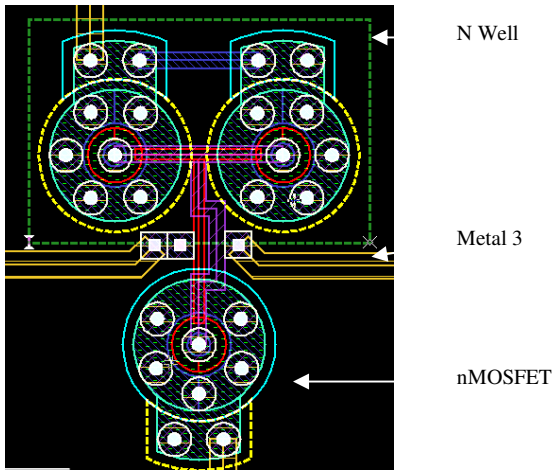

Figure 5: Final CMOS inverter layout implemented with CSM, operating as internal drain bias configuration.

The Glass, Metal 2 and Metal 3 layers were used to implement the PADs. According to the MOSIS design rules, the minimum area for the layer Metal 2 and Metal 3 was 72x72µm², and for the layer Glass was 60x60µm². The Figure 6 presents the layout of the inverter, connected to the PADs, using circular gate transistors.

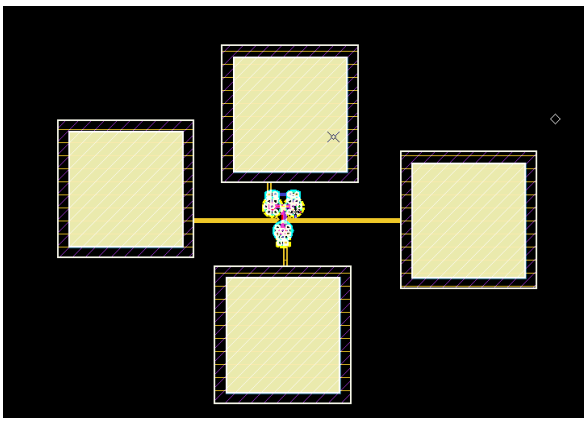

Figure 6: CMOS Inverter layout with PADs.

3. CONVENTIONAL INVERSOR

In order to maintain the conventional geometrical factor (f_g) similar to the circular gate MOSFET, the conventional MOSFET area was calculated to be equal to 24.6x26.4λ², following the MOSIS design rules.

The active contact area was based on CGT active contact area, which is larger than the minimum possible dimension for this technology (2λ). The Figure 7 shows the conventional active contact, covered with a layer of Metal 1.

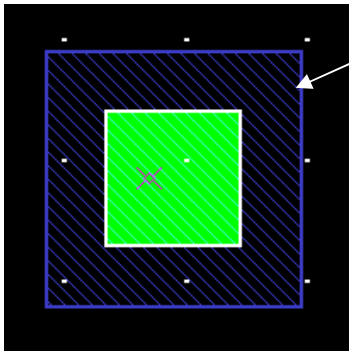

Figure 7: Conventional active contact (internal square), covered by metal 1 layer (external square).

Based on circular gate MOSFET layout and MOSIS with 0.50 µm design rules, the pMOSFET area was calculated in 24.6 x 26.4λ². This area already contains the N Plus area. The Figure 8 shows the conventional pMOSFET layout, where the internal dotted area is doped with P Plus.

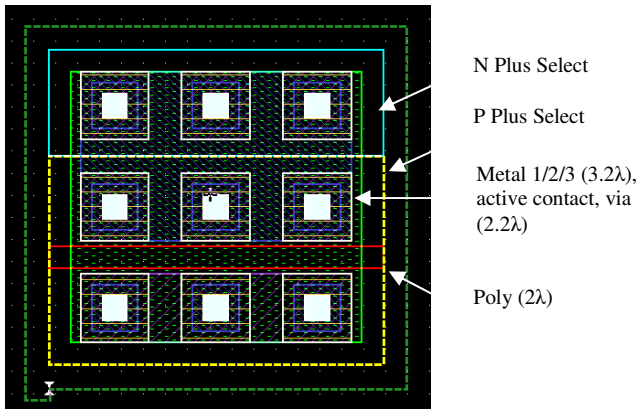

Figure 8: Conventional pMOSFET Layout. Inside the parentheses is displayed the value of the radius of the structure.

After we implemented the rectangular pMOSFET layout, another pMOSFET was generated, by using copy and paste commands, and connected in parallel.

Additionally, minimum dimensions nMOSFET layout was implemented and connected in series with the two pMOSFETs. Figure 9 displays the conventional CMOS inverter layout, which is similar to the circular CMOS inverter.

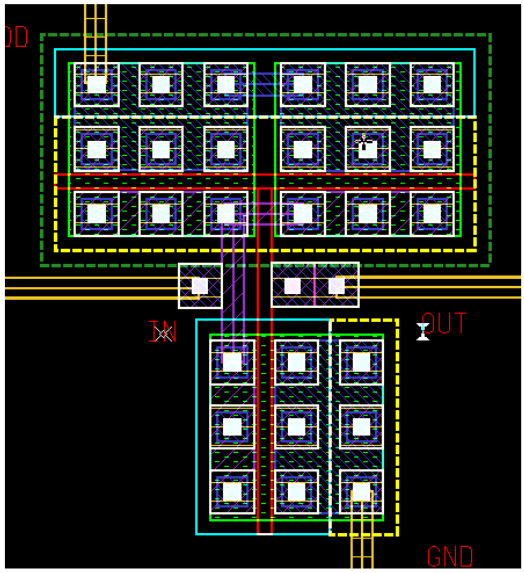

Figure 9: Conventional CMOS inverter without the PADs.

The ports “IN”, “OUT”, “VDD” and “VSS”, were connected to the PADs, using the layer Metal 3, as well. Figure 10 presents the final conventional CMOS inverter layout, connected to the PADs.

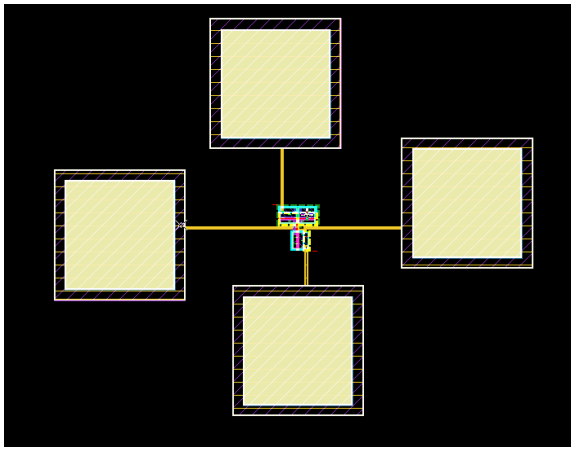

Figure 10: Conventional inverter CMOS layout, connected to the PADs.

Table I shows the circular and conventional CMOS inverters occupied die areas, where A_{conv} and A_{circ} are the conventional and circular CMOS inverter occupied die areas, respectively, Area Gain (%) is the die area gain of circular CMOS inverter has in comparison to the conventional one.

Table I: Areas of the CGT and conventional transistors with L equal to 2λ.

W(λ)	A_{conv} (λ²)	A_{circ} (λ²)	Area Gain (%)
50	1430	1212	15.24%
60	1716	1405	18.11%
70	2002	1614	19.37%
80	2288	1839	19.60%

According to Table I, as the transistors width increases, the area gain of CGT as compared with conventional one, becomes higher.

Table II presents the circular and conventional CMOS inverters die areas, by varying the channel length (L) and maintaining the channel width (W) constant equal to 50λ.

Table II: The CGT and conventional MOSFETs die areas maintaining W fixed.

L(λ)	A_{conv} (λ²)	A_{circ} (λ²)	Area Gain (%)
2	1430	1212	15.24%
3	1480	1271	14.14%
5	1580	1393	11.86%
7	1680	1521	9.48%

Table II shows that, it increasing the channel length of the MOSFETs, the CGT area gain over the conventional one decrease. However, the total area of the CGT is still smaller than the total area of the conventional MOSFET.

4. CONCLUSIONS

This paper describes how to procedure in order to implement circular and conventional gate MOSFETs (n and p types) and CMOS inverters by using MOSIS, 0.50 µm technology, regarding *IC Station* layout editor of Mentor Graphics.

It is possible to conclude that increasing the channel width and fixing the channel length, the CGTs and CMOS inverters implemented with CGT total die areas are smaller than those of conventional counterparts. Besides that, increasing the channel length and maintaining the channel width constant, the CGTs and CMOS inverters implemented with CGT total die areas also are smaller than the conventional counterparts, as well.

Therefore, we believe that, in terms of occupied die area, the CMOS inverters implemented with circular gate transistors is a nice alternative to improve the circuit's compactness.

5. REFERENCES

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