IMPLEMENTING DIAMOND SOI MOSFET LAYOUT

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ABSTRACT

A new layout and structure for SOI MOSFET, was designed and called "Diamond SOI MOSFET (DSM)" (Patent number 018080049795, INPI, Brazil). This name was given due to their hexagonal geometry that uses the corner effect to increase the parallel (longitudinal) electric field over the channel and consequently results a higher drain current (I_{DS}) and transconductance (g_m), regarding the same aspect ratio (W/L), die area and bias conditions, when compared with the Conventional SOI MOSFET (CSM).

1. INTRODUCTION

Silicon-on-Insulator (SOI) MOSFET is a technology that have been widely used in the last years to implement integrated circuits with all kinds of classical planar single-gate and new tridimensional devices (double-gate MOSFETs, triple-gate MOSFETs, and surround-gate MOSFETs), in order to reduce the Short Channel Effects (SCE) and Drain-Induced Barrier Lowering (DIBL) effects and improve current drive [1]. In Figure 1 is shown an example of the Diamond structure, which b and B are the minor and major bases lengths of trapezium formed by the half of the DMS total area; α is the angle formed by the triangle part edges (ED1 and ED2) of the diamond; W is the channel width; L is the effective channel length; t_{si}, t_{ox} and t_{box} are the silicon film, the gate-oxide and buried-oxide thickness, respectively; W/L is the transistor aspect ratio [2]. The parallel electric field over the channel ($\varepsilon_{//}$) of DiamondSM is given by a vectorial sum between each edge of triangular part ($\varepsilon_{//1}$ and $\varepsilon_{//2}$), resulting in a higher $\varepsilon_{//}$ when compared with CSM.

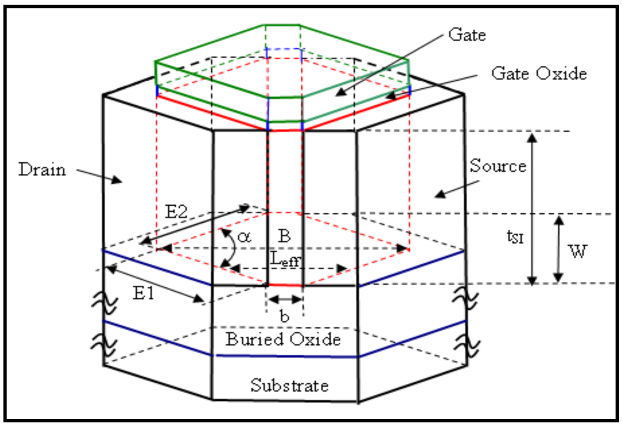

Figure 1 – Diamond SOI MOSFET Structure

When α is closed to 180º, DSM presents similar electrical behavior then CSM. Based on CSM dimensions (W and L), the procedure to obtain the DSM dimensions (b, B, α) is given by: first define a value for b, then use the formula B=2.L-b; and second, use $\alpha=2.[\tan^{-1}(W/B\text{-}b)]$ to obtain the parameter α. To exemplify this method, in table I is shown some examples of CSM and their corresponding DSM.

Is possible to obtain the gate area of DSM by calculating two times the trapezium area which composes the hexagonal shape, which defines: $A_{DSM}=2.\{[(b+B)/2].(W/2)\}=L.W$. This last equation show us that the CSM gate area is equal to DSM gate area.

2. ANALYSIS OF ELECTRICAL AND PHYSICAL BEHAVIOR

Using the parameters shown in Table I for the CSM and DSM devices, the curves $I_{DS}xV_{DS}$ obtained was shown in Figure 2.

Table 1 – CSM and DSM Dimensions.

	CSM			CSM		
#	**W(μm)**	**L(μm)**	**W/L**	**b(μm)**	**B(μm)**	**α(º)**
CSM1/DSM1	6.0	7.0	0.86	1.0	13.0	53.1
CSM2/DSM2	6.0	4.0	1.50	1.0	7.0	90.0
CSM3/DSM3	6.0	2.5	2.40	1.0	4.0	126.9

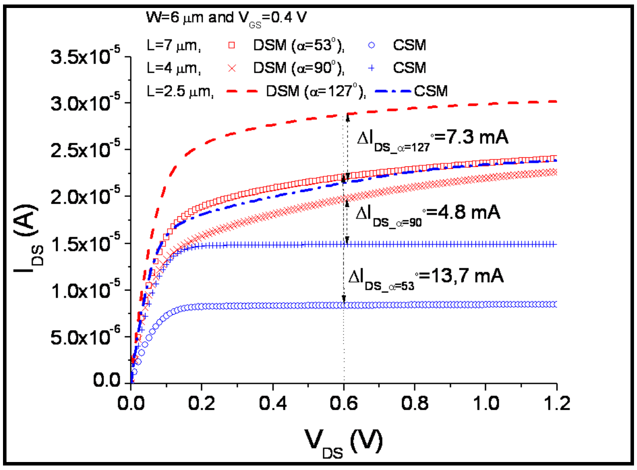

Figure 2 - $I_{DS}xV_{DS}$ curves for CSM and DSM, using V_{GS}=04V

In Figure 2 is possible to observe that ΔI_{DS} is higher for α=53º than for α=90º, which in turn than α=127º. This effect occurs because the electric field density in DSM is higher when α decreases due the higher interaction between the two components of electric field generated by the triangular shape of the interface between channel/source and drain.

When α is equal to 53°, the I_{DS} is 65% larger than CSM counterpart, when operating in the saturation region, and g_m can reach a value 123% higher than the CSM.

In Figure 3 is shown a simulation of the total current density for DSM (a) and CMS (b) in the saturation region for V_{GS}=0.4 V of devices CSM1 and DSM1 (depicted in Table I).

Analyzing Figure 3 is possible to observe that in the DiamondSM, the current density is higher in the centre than in the edges of the hexagonal structure, which suggest us a new future work regarding breakdown and ESD.

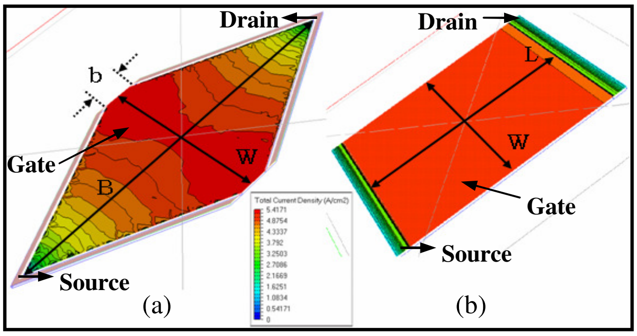

Figure 3 – Total current density for DSM and CSM devices

3. LAYOUT IMPLEMENTATION

The layouts of CSM and DiamondSM were made using the L-edit layout editor (Tanner EDA) [3], by using design rules of Universitè Catholique de Louvain (UCL), Belgium, where they are being fabricated. For this project, four masks were used to implement these devices: active, polysilicon, contacts, and metal.

In Figure 4 is shown an example of these layouts. In Figure 4.a presents a CSM layout (gate rectangular geometry) and in Figure 4.b displays the correspondent DSM. In both layouts the following parameters were used: W = 12 µm; L = 20 µm; b = 2 µm; B = 38 µm; α = 36.9°.

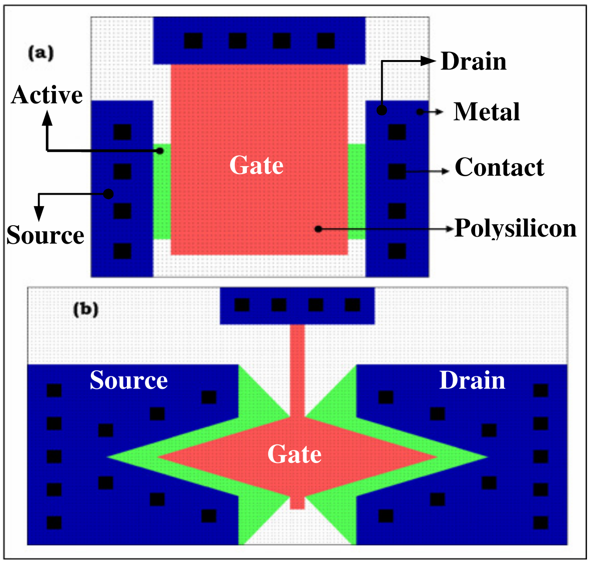

Figure 4 - Layout implementation, Conventional SOI nMOSFET and the corresponding DSM

4. CONCLUSIONS

This article presents a new structure called Diamond. With this new device is possible to obtain a higher drain current in comparison with CSM keeping the same area and aspect ratio.

When the α angle is equal to 53° is possible to obtain 65% of drain current improvement when compared with CSM.

5. REFERENCES

[1] S. P. GIMENEZ, “Diamond SOI MOSFET: A New Drain and Source/Channel Interface Layout to Improve Drain Current”, EUROSOI Fifth Worksho of the Thematic Network on Silicon-On-Insulator Technology, Devices and Circuits, Goteborg Sweden, pp. 87, 2009.

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[3] Software L-edit The Layout Editor, Tanner EDA Version 7.12, 1988.