CMOS FLASH A/D CONVERTER BASED ON THE QUANTIZATION OF THE THRESHOLD VOLTAGE

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ABSTRACT

A flash analog-to-digital converter (ADC) implementation based on the quantization of the threshold voltage of CMOS inverters has been designed for high speed, low voltage, and low power system-on-chip (SoC) applications. The reference voltages for this flash ADC are set internally in the inverters, avoiding the usage of resistive voltage dividers. This technique is called Threshold Inverter Quantization (TIQ), and it reduces the ADC chip-area and power consumption, as compared to traditional flash ADC implementations. To demonstrate the concept, a 4 bit TIQ flash ADC with Gray Code output and a sample-and-hold circuit were designed, using design and simulation software available for free on Internet. As other works have not specified how the comparator transistors were implemented, multiples of minimal CMOS inverter transistors were used. This reduces the project and simulation time, as compared to a previous implementation. The layout and simulation results of the ADC are presented for *250 nm* channel length. The chip area is *0.045 mm*^{2} and the conversion time achieved is under *20 ns*, down to 5 *ns*, depending on the sample and hold circuitry.

1. INTRODUCTION

With the system-on-chip (SoC) trends, analog-to-digital converters (ADCs) are forced to be integrated with other digital circuits on the same chip. Thus high resolution and speed, low voltage and power, are the new challenges in ADC circuit design. Among the available ADC architectures, the Flash one gives the fastest conversion speed, although with an exponentially growing chip-area. In this paper was used the Threshold Inverter Quantization (TIQ) approach, based on systematic transistor sizing of multiples from the basic CMOS inverter projected transistors [5]. Eliminating the resistor array from conventional Flash ADC implementations, this technique can achieve reduced ADC chip-area and power consumption, making it suitable for battery-powered applications.

2. TIQ FLASH ADC ARCHITECTURE

From the resistive flash ADC implementation, only the encoding blocks can be used. The main difference between the resistive and the TIQ techniques comes from how the reference voltages are set. In the resistive implementation, a resistor array is used to form the reference voltages and a repeated comparator cell is used to compare the input voltage with the reference voltages to generate a thermometer code. To avoid high DC power consumption, this resistor should have a high value, implying a big chip-area occupied. In the TIQ implementation, instead of a repeated comparator cell, each comparator is uniquely designed to set its reference voltage internally [5]. Avoiding the use of a resistive array, the DC power component is minimized and there is power consumption peaks only when the transistors switch, demonstrating power consumption benefit. Following the comparator block comes a gain stage, the '01' code generator and a binary encoder. Like the resistive flash implementation, the TIQ one has the disadvantage of exponentially growing chip-area, $2^n - 1$ TIQ comparators for n-bit resolution, but as a resistor can be accurately fabricated, the threshold voltages of CMOS inverters suffers a great influence of fabrication parameters variation. Some others techniques, like the pipeline, could be used together to split the ADC in two or more parts, reducing the chip-area, but making the conversion slower. A 4 bit TIQ ADC with Gray Code output and ROM type encoder was designed and simulated using the parameters of the AMS C35B4C3 technology for a 500 *nm* channel length.

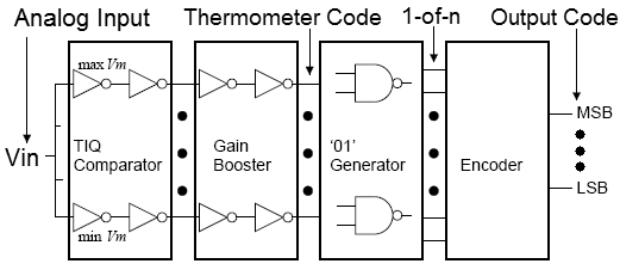

Fig. 1. Block diagram of the TIQ ADC

2.1. TIQ comparator

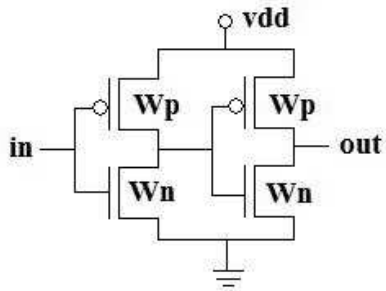

Fig. 2. TIQ comparator schematic

The TIQ comparator is a series combination of two CMOS inverters, with the same transistor channel width (Wn/Wp) relation. Its threshold voltage can be obtained equaling the currents thru both nMOS and pMOS

transistors, assuming same channel length (Ln = Lp) and oxide capacitance (Cox) and given µn and µp mobility parameters, available from the technology book [5].

$$Vm = \frac{\sqrt{\frac{\mu_p . W_p}{\mu_n . W_n}} . \left(V_{DD} - \left|V_{Tp}\right|\right) + V_{Tn}}{1 + \sqrt{\frac{\mu_p . W_p}{\mu_n . W_n}}}$$

So, varying the channel widths (Wp and Wn) values, the threshold voltages can be set to the reference voltages calculated. The major challenge here is: the threshold voltage is sensible to fabrication parameters variation, such as variations on μ_p and μ_n due to the process itself, it suffers also influence of power supply and temperature, it is not linear with Wn and Wp, and resistors can be very well designed and characterized, so the errors at CMOS inverters threshold voltages are higher than the matching errors at resistors, making a possible post-calibration required.

There are two methods available: Random Size Variation (RSV) and Systematic Size Variation (SSV). As SSV shows less non-linearity errors [6], the designed ADC used this method. And the following procedure was used:

1. Design a minimal size inverter, so that: Vm = Vdd/2;
2. Set the safe input analog range (AR), with AR_{max} = Vdd – (|Vtp| + Vtn);
3. Calculate the least significant bit (LSB) voltage: LSB = AR / (2^n – 1) (for a n-bit ADC);
4. Calculate the reference voltages (Vref) from: Vref(k) = Vmin + k*LSB, 0 < k < 2^n - 2;
5. Using calculation software, create a table of threshold voltages using multiples of the projected minimal inverter transistors as variables and search in it the sequence of the desired reference voltages, following a diagonal line (SSV method), selecting the number of transistors used for each reference voltage.

As previous works do not show how the TIQ comparators transistors were implemented, instead of using one big transistor, multiples of the minimal CMOS inverter transistors were connected in parallel, to form a big one [2,3,4,5,6]. This implementation tries to reduce the variation of fabrication parameters, since a repeated small good transistor has less variation then a bigger one [1]. The projected minimal inverter has (for a 2λ = 0.5 µm parameter) Lp = Ln = 2λ = 0.5 µm, Wn = 3λ = 0.75 µm and Wp = 10λ = 2.5 µm, with 1.641 V as threshold voltage, where λ is the design rule parameter.

2.2. Gain stage

It is basically an array of 2^n – 1 gain cells, each formed by two minimal inverters in a series combination. They make the generated thermometer code (from the comparators block) sharp, but introduce delay.

2.3. ‘01’ code generator

This encoder stage is used to transform the thermometer code into a “1-of-n” code, setting the output related to the position of the thermometer edge. To this stage, a cell was designed using a 2 inputs NAND gate with two inverters as shown in Figure 3. Such gates have the following description:

- NAND: Ln = Lp = 0.5 µm; Wn = 0.75 µm and Wp = 1.5 µm;
- Inverters: Ln = Lp = 0.5 µm; Wn = 0.75 µm and Wp = 2.5 µm

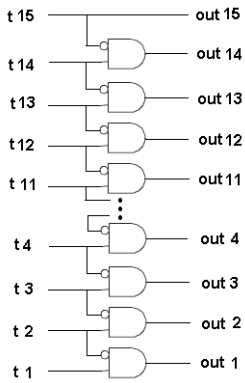

Fig. 3. ‘01’ code generator

2.4. Binary code generator

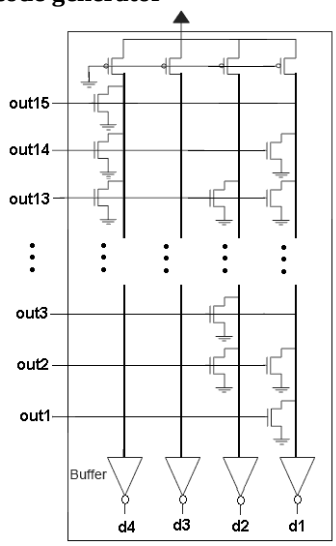

Fig. 4. Binary word generator, ROM memory

The set line from the ‘01’ code is used as the address of a read-only memory (ROM), which generates the desired output code. A Gray code was used as binary output, trying to minimize the eventual errors from words transitions. The ROM project showed in Figure 4 has four pre-charge pMOS transistors, four inverters, and the presence of one nMOS transistor indicates a ‘1’ on the output word. Other approaches, like the Fat Tree

Encoder [6] can be also used to achieve higher rates. The designed ROM has the following characteristics:

- Pre-charge pMOS transistors: Lp = 2λ = 0.5 µm, Wp = 3λ = 0.75 µm;
- nMOS transistors: Ln = 0.5 µm, Wn = 0.75 µm
- Inverters: Ln = Lp = 0.5 µm; Wn = 0.75 µm and Wp = 2.5 µm

4. SAMPLING CIRCUIT

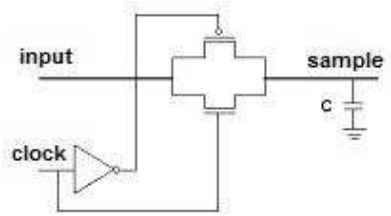

Fig. 5. Track-and-hold schematic

The sampling circuit was a basic track-and-hold circuit, composed by a MOS switch cascaded with a capacitor and an inverter. This is not the optimal approach, because it loads the input with the sampling capacitor. Another approach should be used in the future works. The designed circuit has a time constant τ near 2.5 ns, providing a charge/discharge time of 10 ns. The projected sizing and parameters (using the technology parameters) of the circuit was:

- Capacitor: 420 x 200 λ² (5250 µm²) ≈ 1 pF
- Comparators input capacitance ≈ 1.5 pF
- MOS Switch: Ln = Lp = 0.5 µm, Wn = 6 µm, Wp = 18.75 µm

5. LAYOUT AND SIMULATION RESULTS

Using the AMS C35B4C3 technology parameters, the Electric VLSI Design System (available for free at Static Free Software website) layout tool, and the Spice-Opus simulator, also available for free on Internet, the layout designed is shown in Figure 6, and some simulation results come below. Considering the nominal case as V_{DD} = 3.3 V and T = 27 °C, the maximal conversion rate, power consumption, static performance parameters [6], and the influence of temperature and power supply variation were analyzed.

At Table 1 the characteristics of the designed 4 bit Flash TIQ ADC are shown, using the design rule parameter λ equal to 0.25 µm. At Table 2 the projected reference voltages, the simulated threshold voltages, the output, and the differential non-linearity error (DNL) and the integral non-linearity error (INL) are shown for the nominal case. And at Table 3, the deviation of the converter static parameters, such as gain and offset errors, DNL, INL, analog input range (AR), least significant bit voltage (LSB), and power consumption, due to ± 5% power supply variation and high and low temperatures (85 °C and -40 °C) are presented.

But, we must yet consider a Monte Carlo analysis to make an effective comparison of the influence of fabrication parameters variation, such as the transistors mobility parameters (µ) and threshold voltages (Vt), on the CMOS inverters threshold voltages.

Making all the output bits go from "0" to "1" as shown in Figure 7 show that a maximal 200 MSPS conversion rate for the ADC can be achieved, considering an ideal sample-and-hold circuit. But, for a complete system, the delay in long lines should be considered using a more powerful design tool to the maximal conversion rate calculation.

The time constant of the projected track-and-hold circuit is about 10 ns, so a sampling frequency of 50 MHz (Ts = conversion period = 20 ns) can be achieved. With a 25 MHz sampling frequency (Ts = 40 ns) due to the Nyquist rate we may convert a signal with 12.5 MHz frequency. The sampled voltages in Figure 9 were 1.05 V and 2.5 V, which correspond to the words 0011 and 1000 in gray code, as expected as the conversion results.

Table 1. Designed TIQ ADC characteristics

Resolution	4 bits
CMOS technology	0.35 µm
Chip-area	0.0448 mm² (2λ = 0.5 µm)
LSB voltage	100 mV
Input operation range	0.891 V < Vin < 2.391 V
Max sample rate	200 MSPS
Max power consumption	19.6 mW
DNL_{max}	0.26 LSB
INL_{max}	1.07 LSB
Charge/Discharge time	10 ns

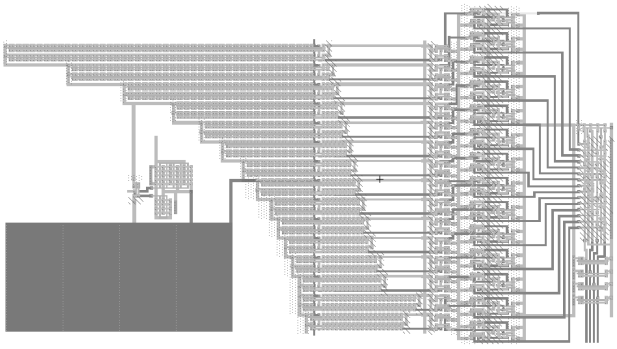

Fig. 6. The 4 bit TIQ Flash ADC generated layout, with sampling circuit. 1143 x 627 λ² = 0.0448 mm²

Table 2. Comparison between the project and simulation

k	Vref (V)	Vsim (V)	Word	DNL (LSB)	INL (LSB)
14	2,385	2,391	1000		1,07
13	2,277	2,287	1001	0,06	1,01
12	2,172	2,183	1011	0,04	0,97
11	2,060	2,067	1010	0,17	0,80
10	1,960	1,967	1110	0,01	0,79
9	1,854	1,868	1111	0,00	0,79
8	1,747	1,753	1101	0,16	0,63
7	1,641	1,648	1100	0,06	0,57
6	1,535	1,527	0100	0,22	0,35
5	1,429	1,443	0101	-0,15	0,50
4	1,322	1,347	0111	-0,03	0,54
3	1,216	1,222	0110	0,26	0,27
2	1,110	1,098	0010	0,25	0,03
1	1,004	0,997	0011	0,03	0,00
0	0,897	0,891	0001	0,06	-0,06

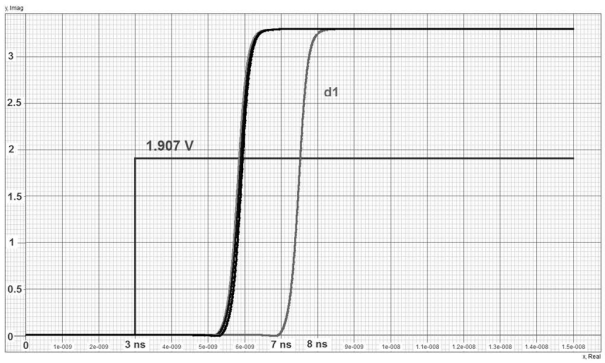

Fig. 7. Delay analysis ([d3,d2,d1,d0] x time) showing a maximal 4,5 ns delay for the bit d1.

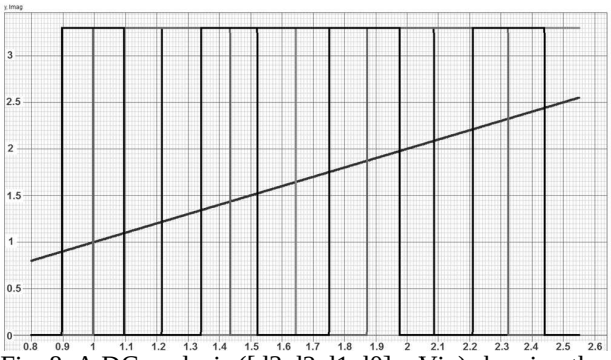

Fig. 8. A DC analysis ([d3,d2,d1,d0] x Vin) showing the threshold voltages for a DC input from 0.8 V to 2.55 V

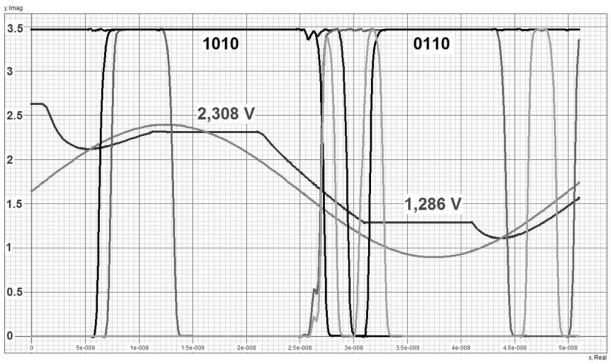

Fig. 9. A Transient analysis ([d3,d2,d1,d0] x time) showing a example of conversion using the track-and-hold circuit designed. fsgn = 20 MHz, Fs = 50 MHz, amplitude = 1.5 Vpp

Table 3. Influences of the temperature and power supply

	Nominal	Vdd	Vdd	Temp	Temp	Max Deviation
		1,135 V	1,465 V	- 40 °C	85 °C	
AR (V)	1,500	1,418	1,668	1,450	1,644	11,18 %
LSB (V)	0,100	0,095	0,111	0,097	0,110	11,18 %
Offset (LSB)	-0,06	-0,28	0,26	0,22	-0,22	0,324
Gain (%AR)	0,86	-4,69	12,14	-2,49	10,55	11,277
DNL (LSB)	0,26	0,20	0,38	0,20	0,36	46,15 %
INL (LSB)	1,07	0,52	3,09	0,85	2,36	2,02
Power (mW)	19,6	17,0	22,2	23,8	17,4	21,43 %

6. CONCLUSION

A new Flash ADC implementation called TIQ (Threshold Inverter Quantization), which eliminates the use of a resistive array, was used to design a 4 bit analog-to-digital converter (ADC), using Gray Code as output binary words. The AMS C35B4C3 technology parameters were used to generate the layout and to simulate it, using a 2λ design parameter equal to 0.5 µm.

The results obtained from the simulations show a maximal 200 MSPS conversion rate for the ADC block itself, with nominal 20 mW power consumption, and a conversion rate higher as 50 MHz when using the designed track-and-hold circuit. Therefore this approach of an ADC is suitable for System-on-Chip (SoC) projects, where reduced area and power, together with high speed conversion are the main requirements, although the track-and-hold circuit was only one preliminary experiment.

As future steps, the projected converter should be redesigned to improve its area and performance parameters, using multiples of the technology minimal nMOS and pMOS transistors; a Monte Carlo analysis could be performed to analyze the process parameters variation influence on the reference voltages; and a proper sample-and-hold circuit should be projected.

7. ACKNOWLEDGMENTS

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8. REFERENCES

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