IMPACT OF THE HALO REGION ON FLOATING BODY EFFECTS IN TRIPLE GATE FINFETS

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ABSTRACT

This paper investigates the impact of the HALO region on the floating body effect (FBE) in triple gate FinFETs. This study was based on the analysis of threshold voltage, capacitance, transconductance and drain current switch-off transients. In the studied fin width range, the second peak amplitude transconductance reduces for HALO devices. The transient time increased substantially for devices without a HALO region, demonstrating that these devices are more susceptible to the FBE influence.

1. INTRODUCTION

The reduced gate control of the channel region has been the main limitation associated with a geometry reduction in SOI MOSFETs. Multiple-gate architectures have been proposed to improve the gate control on the channel region, minimizing the short channel effects and consequently increasing the current drive of these devices.

Among the different multiple-gate structures the triple gate FinFET devices are a strong candidate for the planar SOI technology [1] succession. In these devices the gate is placed around the silicon island, named "fin" [2,3]. Depending on the "fin" dimension the current flows predominantly along the top or the lateral gates [4].

Figure 1 shows schematically a triple gate FinFET device, emphasizing its geometric parameters, where W_{fin} is the fin width, h_{fin} the fin height and L the channel length.

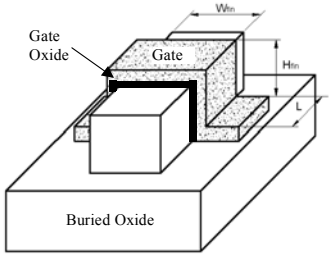

Figure 1 - Schematic of a FinFET device showing the relevant dimensions.

Another alternative to prevent the short channel effects is the use of a HALO region. This region with higher doping concentration is located near the drain and source regions [5].

The channel width (W_{fin}) is an important geometric parameter for the electrical behavior of these devices. Previous studies reported an increase of the series resistance with a W_{fin} reduction [6]. The W_{fin} variation impacts on the output conductance, on the voltage gain [7] and on the analog circuits performance [8,9].

Body contacts are not used anymore in the large-scale integration of a SOI technology. If the body region is not biased the floating body effect (FBE) phenomenon increases, which changes the performance of these devices [10]. Normally, the FBEs are stronger in partially depleted devices but they can also be observed in fully depleted devices when the back interface is operating in accumulation [11].

The drain current transient is one of the FBEs, occurring for a step change in the transistor front gate voltage from "on" to "off". This phenomenon is due to the variation of the maximum depletion region that follows the body potential occurring just after the front gate bias change. The steady state of the body potential and consequently the drain current is obtained from the generation-recombination process that reestablishes the balance of the majority carries density in the device body region [10-12].

When in n-channel devices the front gate bias changes from the strong inversion to accumulation (switching off), holes are generated to build-up the depletion region, resulting in a reduced maximum depletion region width corresponding with the new front gate bias. This generation process has an impact on the threshold voltage, which is initially increased, but then evolutes back to its steady state value. The inverse case happens when the front gate changes from accumulation to strong inversion (switching on). In that case the holes recombine to increase the depletion region and to reach a smaller value of the threshold voltage, corresponding to the steady condition.

The main goal of this work is to analyze the influence of the presence of a HALO implantation region on the floating body effects in triple gate FinFETs by investigating threshold voltage, capacitance, transconductance and switching-off transient.

2. FinFET FABRICATION

The triple-gate FinFETs were fabricated on SOI wafers with 145 nm buried oxide thickness, following the process described in Ref. [13]. The top silicon layer thickness, which is the fin height (H_{fin}), is patterned to a thickness of 60 nm. After the silicon film definition, a 1 nm thick interfacial thermal oxide was grown, followed by the atomic layer deposition (ALD) of 2 nm HfO_2. The gate stack is completed with a 5 nm thick TiN ALD film and a 100 nm polysilicon layer. No channel doping is applied during the processing, resulting in natural doping devices (N_a=1x10^{15} cm^{-3}).

3. MEASUREMENTS AND DISCUSSION

The measurements were performed on devices with a channel length (L) of 10μm and a mask width (W_{fin}) varying between 1 and 20 μm. The experimental curves were obtained with a HP4156 semiconductor parameter analyzer.

Due to the low doping of body region (N_a) and to the small height fin (h_{fin}), it was not possible to observe floating body effects for a back gate voltage of V_{GB}= 0V. In this case the devices were fully depleted and to observe the FBEs it was necessary to bias the back interface in strong accumulation. In order to determine the voltage resulting in a back interface accumulation state, the second derivative of the drain current I_{DS} in function of V_{GF} curve ($d^2(I_{DS})/d^2(V_{GF})$) for devices (Figure 2A) with and (Figure 2B) without HALO region was analyzed.

Figure 2A shows that only one peak of the second derivative drain current is observed, related to the front threshold voltage. However, the two threshold voltages observed for devices without HALO, as shown in Fig. 2B for $V_{GB} \geq 0$ V, are related to the back and front inversion.

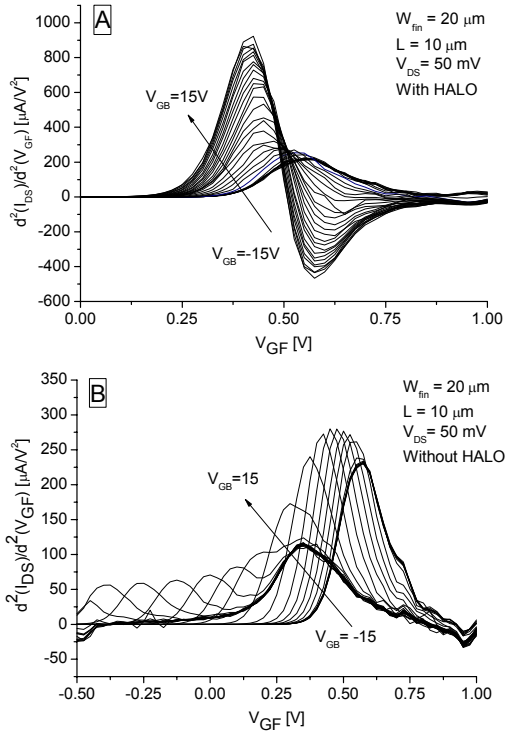

Figure 2. d^2I_{DS}/dV_{GF}^2 vs. V_{GF} experimental curves for different V_{GB} and for devices (A) with and (B) without HALO.

Figure 3A presents the threshold voltage as a function of the back gate voltage for devices with and without HALO implantation. Devices without HALO have the back interface in inversion for V_{GB}=0V, while it is in depletion for devices with HALO. The back interface accumulation appears for the same back gate voltage for devices with and without HALO. The threshold voltage (V_T) as a function of the channel width with a back gate voltage of V_{GB}=0 and –20V is presented in Figure 3B. The fact that devices without HALO present the back interface inverted for V_{GB}=0V, results in a threshold voltage reduction for all channel widths analyzed. For V_{GB}=-20V both devices are certainly operating in the accumulation regime and in that case a lower threshold voltage variation is observed.

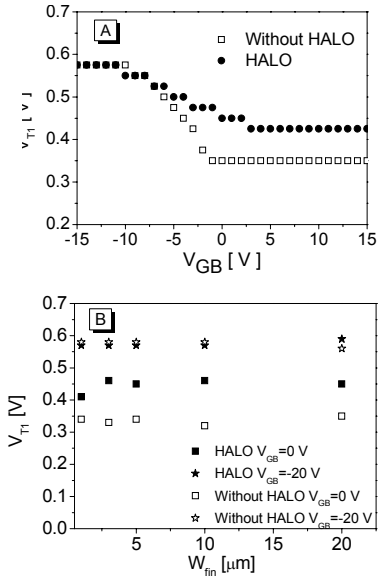

Figure 3 – (A) Experimental front threshold voltage vs. back gate voltage and (B) vs. channel width for V_{GB}= 0, –20V for devices with and without HALO.

ATLAS three-dimensional numerical simulations [14] were performed in order to analyze the HALO implantation influence. The triple gate nMOS FinFET structures used in this paper were simulated with the following parameters: W_{fin}=10 μm, L=1 μm, TiN gate material with work function Φ_M = 4.7 eV, EOT=2 nm, t_{oxb}=145 nm, H_{fin}=60 nm, N_a=1x10^{15} cm^{-3}, LDD extension doping concentration N_D=N_S=1x10^{19} cm^{-3} and with front Q_{ox1} and back Q_{ox2} oxide charges negligible. A doping concentration of N_h=1x10^{18} cm^{-3} was considered for devices with a HALO region.

Figure 4 shows the body potential along the device extracted at several depths in the fin region. The potential variation in the HALO region is significantly smaller than in the middle of the channel region due to the high doping concentration in the HALO region. This explains why a higher voltage is required to change the back interface condition in HALO devices.

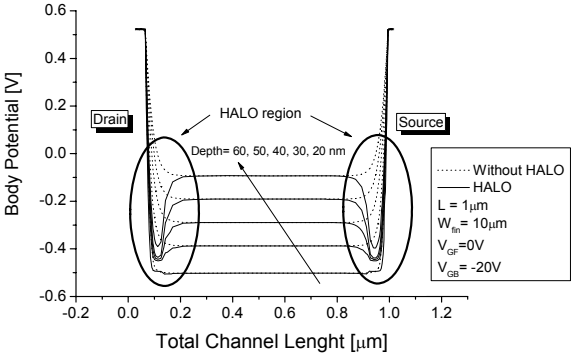

Figure 4 - Body potential along the device at several fin height depths.

Figure 5 presents the simulated gate to channel capacitance (C_{GC}) in function of V_{GB} and its second derivative for V_{GF}=-1V (ensures that the first interface is in accumulation). The maximum peak of the second derivative represents the back gate voltage that starts the back interface inversion, with the first interface accumulated. The device with a HALO region requires a higher V_{GB} =V_{T2}= 11.4V to invert the back interface.

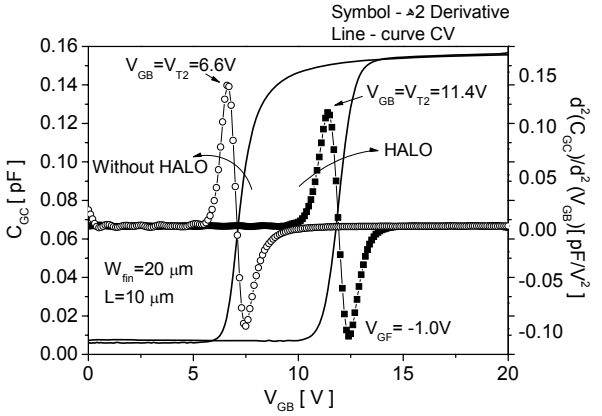

Figure 5 - Simulated C_{GC} versus V_{GB} for FinFET devices with and without HALO and V_{GF}=-1V.

Figure 6 presents the measured C_{GC} vs. $V_{GF,}$ which were performed with HP4280 LCR Meter at 1 MHz using the HP4140 Picoamperimeter to bias the substrate (V_{GB}). It is known that in C-V curves when V_{GB} is biased with a voltage that inverts the back interface, a level in the curve is observed for a V_{GF} that accumulates the first interface [15]. As observed in Figure 5, for V_{GB}=5V only the devices without HALO show an increase in the minimum capacitance (due to the back interface inversion). Therefore, for HALO devices it is necessary to increase V_{GB} to around 15V to

observe the same condition of the back interface, showing that the influence of the back gate bias is higher for devices without HALO.

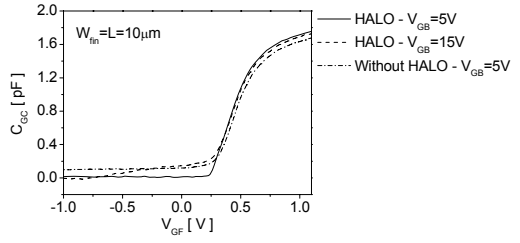

Figure 6 - Experimental C_{GC} versus V_{GF} curve for devices with and without HALO and different V_{GB}.

Devices with thinner gate oxide can be affected by FBEs associated with the direct tunneling through the gate oxide. This phenomenon can be explained by the electron tunneling from the valence band (EVB) that occurs for higher gate voltage, injecting a substantial amount of majority carriers inside the body region. As a result an increase is observed in the body potential and a consequent decrease in threshold voltage as can be observed by the second peak in the transconductance curve.

Figure 7 shows the drain transconductance normalized by the channel width as a function of the front gate voltage, for devices with and without HALO region. The higher maximum transconductance value observed in devices with higher W_{fin} is due to the higher mobility in the superficial [100] crystallographic plane than in the lateral [110] sidewalls. A reduction of the second gm peak amplitude is observed in both HALO and non HALO devices for devices with a smaller width. This can be a result of the higher lateral gate coupling in narrower FinFETs [16], which minimizes the FBE. At the same time, when comparing devices with the same W_{fin}, a higher reduction in the second peak amplitude of the transconductance can be noted for structures with HALO, implying that the presence of this region reduces the body potential variation.

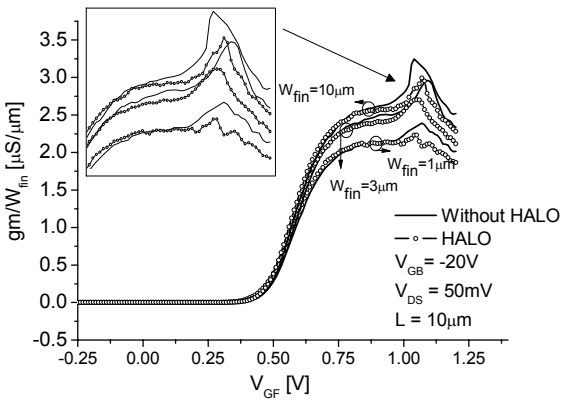

Figure 7 – Normalized drain transconductance as function of gate voltage for devices with and without HALO and different channel widths.

Through the threshold voltage, capacitance, and transconductance analysis it was possible to define the bias condition of the FinFET devices, in order to observe the drain current transient. In the same way as in the case of the transconductance second peak, the drain current transient can only be observed for the back interface accumulation condition. The following analysis uses a back gate voltage of V_{GB}= –20V, because for this condition no variation in threshold voltage was observed for both devices, with and without HALO, in the W_{fin} range studied.

Figure 8 shows the drain current transient normalized by the steady state current value, for devices with L=10μm and W_{fin}=3μm, varying the high level step voltage (V_{Ghigh}) applied to the gate. Similar as previously observed in planar PD SOI nMOSFET devices, for a V_{G_high} above the threshold voltage a higher drain current variation is obtained after the negative gate voltage step. Values of V_{G_high} nearby the voltage that gives the second peak of the drain transconductance curve, decrease the transient until an inversion of the behavior occurs [17]. The transient behavior is due to the majority carriers excess (holes in this case) injected in the body region by the direct gate tunneling. The hole accumulation in the body region results in an potential increase of this region, and a threshold voltage reduction. The body potential and the drain current reach the equilibrium through a recombination process.

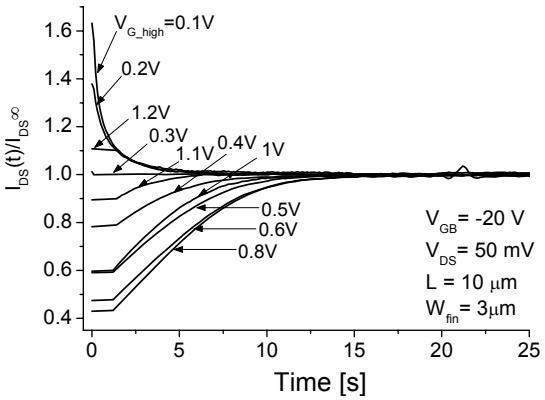

Figure 8 - Drain current transient normalized by the steady state current value, for devices with a channel length of L=10μm and W_{fin}=3μm, varying V_{G_high}.

Figure 9 compares the drain current behavior in function of the gate voltage in devices with and without the HALO region and with different W_{fin}. Devices with HALO present a lower leakage current (V_{GF}=0V) due to the higher built-in potential formed between source/drain and HALO region, which presents a higher doping concentration and a consequently reduction of the current density through the junction.

Just after the application of a negative step voltage at the gate of the transistor (V_{G_high}=0.8V to V_{G_low}=0.3V), the drain current is suppressed and is then gradually increasing with time to the steady state value. This current transient normalized by W_{fin} is presented in Figure 10. Lower drain current transient levels are expected in this case due to the lower current level in the subthreshold region, observed in the devices without HALO. With the decrease of W_{fin} a better gate coupling is observed. This effect reduces the influence of the back interface accumulation region in the body potential variation and can also be observed through the lower transient current levels in devices with larger W_{fin}. This fact suggests that in larger devices the body potential reaches lower values and consequently a higher threshold voltage, which causes a drain current reduction during the transient.

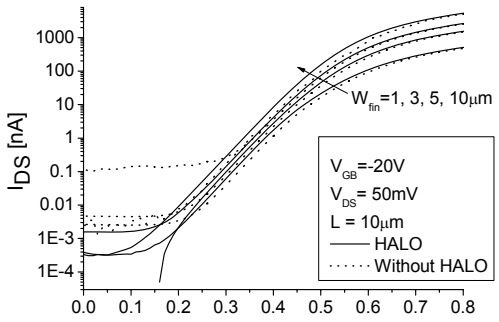

Figure 9 – Drain current as function of front gate voltage for devices with and without HALO region and different channel width.

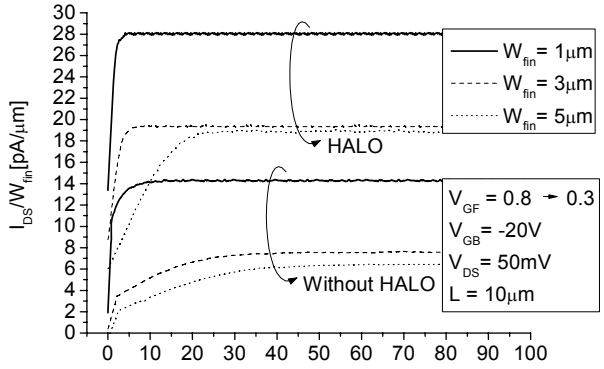

Figure 10 - Drain current transient normalized by W_{fin} as function of the time.

The drain current was normalized by the steady state current value (Figure 11) and from these curves it is possible to obtain the transient time, which is defined as the time necessary for the drain current to reach 90% from its steady state value. Devices with HALO (Figure 11A) and without HALO (Figure 11B), showed a transient time reduction with decrease of W_{fin}. When devices with the same channel width are compared it can be noticed that the transient time increases substantially in devices without HALO region, showing that this type of device presents a strong influence of FBEs. Just after applying the negative step the normalized drain current was lower for devices without HALO when compared with HALO devices. This effect is due to the high body potential variation, in agreement with our previous analyzes.

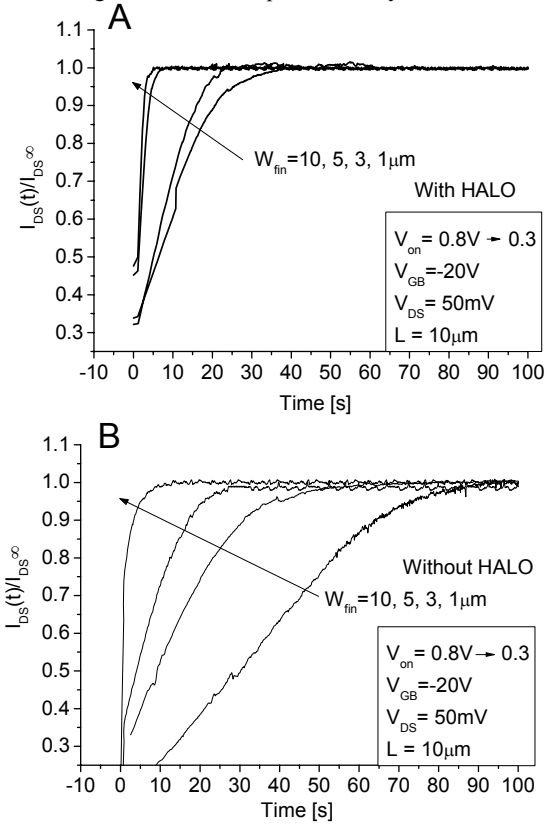

Figure 11– Drain current transient normalized by the steady state current value with W_{fin} variation for devices (A) with and (B) without HALO.

4. CONCLUSIONS

The impact of a HALO implanted region on the floating body effect in n-type FinFET has been investigated. It was demonstrated that the threshold voltage is lower in devices without HALO. Devices with and without HALO showed a reduction in the second peak amplitude transconductance with a reduction of W_{fin}. Comparing devices with the same W_{fin} with and without HALO, it was shown that HALO devices exhibit a lower second peak amplitude transconductance. The HALO devices also exhibited a transient time reduction with a decrease of W_{fin}. The same phenomenon observed in devices without HALO. Therefore, when devices with the same W_{fin} are compared it can be observed that the transient time increases substantially in devices without HALO. Finally, it can be concluded that the devices without HALO are more susceptible to the influence of FBEs.

5. ACKNOWLEDGMENTS

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