EVALUATION OF THE DRAIN LEAKAGE CURRENT BEHAVIOR IN DOUBLE GATE FINFETS

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ABSTRACT

In this study it will shown the drain leakage current behavior and its carriers composition in Double Gate FinFETs (DGFinFETs) devices submitted since room temperature (27 ºC) up to 300 ºC, taking into account the influence of the channel length (L) in the total drain leakage current $I_{DLeak}$ and its composition (electrons and holes). In order to develop this analysis, numerical three-dimensional simulations were performed, where it was observed that the drain leakage current increases as the temperature rises for all simulated devices and $I_{DLeak}$ increases as L reduces. Besides, it was observed that the total drain leakage current $I_{DLeak}$ in DGFinFETs showed to be composed mainly by electrons.

1. INTRODUCTION

The Silicon-on-Insulator (SOI) MOS technology evolving from the classical model, planar, single gate into three-dimensional structures devices with a multiple gates (MuGFETs) devices [1].

Double gate devices have the best conditions to electrostatic control of channel region when compare to planar single gate devices, short channel effects are reduced and smaller dimension for transistor can be achieved with double gate structures [2].

Nowadays there are many applications for SOI MOSFETs and Integrated Circuits (ICs) for high temperature operation up to 300 ºC, such as automotive, aerospace and industry whose have a special demand for then [3, 4]. At high temperatures, the main cause of failure in devices and circuits is due to the leakage current increases on drain/source to channel junctions [3, 4].

Multiple gates devices are the main promises to advance the limits of the integration scale and have attracted interest in several research groups [5, 6].

Then, looking for these premises, in this study the drain leakage drain current and its carriers will be analyzed and discussed in DGFinFETs SOI nMOS devices.

2. DOUBLE GATE FINFET CHARACTERISTICS

The Double Gate FinFET devices (DGFinFET) used in all three-dimensional simulations is showed in Figure 1. Its characteristics are: the Fin width ($W_{FIN}$) is 120 nm, the Fin height ($H_{FIN}$) assumes 150 nm, the buried oxide ($t_{BOX}$) and gate oxide ($t_{OX}$) have 145 nm and 2 nm thickness, respectively. The channel length range analyzed is changes from 100 nm up to 1 µm. The channel region has a p-type doping concentration $N_A=1x10^{20}$ cm$^{-3}$ while source and drain regions are a n-type with doping concentration $N_D=1x10^{20}$ cm$^{-3}$, characterizing a n-channel Double Gate FinFET.

![Double Gate FinFET transistor structure.](image)

In order to analyze $I_{DLeak}$ at high temperatures, all devices were biased in the linear region, i.e., for the drain voltage $V_{DS}$ fixed at 25 mV. The gate voltage $V_{GS}$ versus drain current $I_{DS}$ curves were obtained in all temperature range for $-0.5 \leq V_{GS} \leq +1.2$ V.

In order to edit the DGFinFETs devices, it was used DEVEDIT3D [7], and all three-dimensional numerical simulations were performed using ATLAS [7].

3. THREE-DIMENSIONAL SIMULATION RESULTS

The results presented were obtained through three-dimensional numerical simulations, performed with the device simulator ATLAS.

In order to study the drain leakage current $I_{DLeak}$ it is necessary to obtain the drain current $I_{DS}$ as a function of the gate voltage $V_{GS}$ curves, for all temperature range analyzed, for an constant voltage applied between drain and source $V_{DS}=25$mV, and for the gate voltage from $V_{GS}=-0.5$ V up to $V_{GS}=+1.2$ V.

Figure 2 shows some results concerned to the $I_{DS}$ x $V_{GS}$ curves, at high temperatures, for a DGFinFET SOI nMOSFET with $L=500$ nm. From these results is possible to note that as the temperatures increases, the subthreshold slope decreases. Besides it, in the triode region ($V_{GS} > 0.5$ V) $I_{DS}$ reduces due to the mobility reduction as the temperature rises. Similar results are observed for all L range analyzed along this paper.
In order to extract the total drain leakage current $I_{DL,\text{leak}}$, it was necessary to adopt a $V_{GS}$ condition for it. Then, after analyzing all $I_{DS} \times V_{GS}$ curves, it was decided that $I_{DL,\text{leak}}$ can be extracted for $V_{GS} = -0.5$ V, where $I_{DL,\text{leak}}$ tends to be almost constant at high temperatures.

The results of $I_{DL,\text{leak}}$ extracted for all DG FinFETs analyzed are described in Figure 3, showing that the drain leakage current $I_{DL,\text{leak}}$ increases as the temperature rises, as expected.

From the results presented in Figure 3, it can be seen that for a given temperature, the channel length $L$ reduces there is an increase of $I_{DL,\text{leak}}$, whose effect is observed for all temperature range studied along this work. On the other hand, $I_{DL,\text{leak}}$ difference observed between the devices reduces as the temperature increases.

Otherwise, analyzing $I_{DL,\text{leak}}$ as a function of $L$, it can be seen that for the same temperature as $L$ reduces, $I_{DL,\text{leak}}$ increases as it can be seen in Figure 4. Similar behavior is also observed for all temperature range evaluated.

In order to understand $I_{DL,\text{leak}}$ behavior as a function of $L$ and temperature, the drain leakage current densities and its composition (holes and electrons densities) were investigated into the silicon film volume of DG FinFETs, as it will be described below.

4. DRAIN LEAKAGE CURRENT ANALYSIS

The total drain leakage current density $J_{DL,\text{leak}}$ is obtained from the structure generated by the simulator, previously polarized in the leakage region (for $V_{GS} = -0.5$ V) as described above, and through a cut view in the middle of the FinFET height of this structure, given by $H_{Fin}/2$ and is extended across the width $W_{Fin}$ of the transistor, i.e., since from the Gate 1 and 2/silicon film interfaces, as it can be seen in Figure 5.
As the DGFinFET channel length reduces, as presented in Figure 7, there is a significant \( J_{\text{TL}_{\text{Leak}}} \) increase, but similar behavior in the distribution of the total drain leakage current is maintained, i.e., the most part of it flows around the middle of \( W_{\text{Fin}} \) and it increases as the temperature increases.

Then, in order to understand \( J_{\text{TL}_{\text{Leak}}} \) behavior as a function of the temperature and \( L \), the total drain leakage current composition (carriers) was investigated to observe how electrons and holes contribute for \( I_{\text{D}_{\text{Leak}}} \) in these analyzed conditions. In this way, Figure 8 shows the total drain leakage current density and its carriers results concerning to DG FinFET operating at 300 °C and for \( L \) being 1µm.

From the results presented in Figure 8, it is possible to observe that when the device is operating at 300 °C, the total drain leakage current is composed mainly by electrons \( J_{\text{Electrons}} \). Besides it, note that near the gate interfaces the density of holes is more significant when compared to the rest of the silicon film width, due to negative bias applied in both gates (\( V_G = -0.5 \) V), which naturally leads to accumulation of holes at these interfaces. In the median region of \( W_{\text{Fin}} \) the density of holes \( J_{\text{Holes}} \) is around three orders of magnitude lower.

Similar results were also observed when \( L \) assumes 500 nm and 100 nm, as shown in Figures 9 and 10, respectively. But in these cases, it is important to mention that \( I_{\text{D}_{\text{Leak}}} \) is composed mainly by electrons \( J_{\text{Electrons}} \) but \( J_{\text{Leak}} \) increases as \( L \) reduces. Besides it, as \( L \) reduces, the drain leakage current measured around the Gate 1 and 2 interfaces becomes higher and its composition is given also mainly by electrons, reinforcing that as the channel length reduces, \( I_{\text{D}_{\text{Leak}}} \) increases and its main carrier is given by electrons.
For lower temperatures, similar results were observed for all DGFinFETs SOI nMOS evaluated in this work. When the DGFinFETs are analyzed at room temperature, the composition of the total drain leakage current is similar those observed at higher temperatures, for all devices with different lengths of channel. But in particular, when L assumes 1 µm, it is possible to see that $I_{DLeak}$ components (holes and electrons) are of the same order of magnitude and both contribute significantly to $I_{DLeak}$, as it can be seen in Figure 11.

Three-dimensional numerical simulations were performed to assist in understanding the drain current composition and its distribution in DGFinFETs, as a function of the temperature and the channel length. As expected, the drain leakage current $I_{DLeak}$ is highly dependent on the temperature of operation, being higher when the DG FinFET devices are submitted at high temperatures. The results show that as L decreases, for the same conditions, $I_{DLeak}$ increases and similar behavior is also observed for the same channel length as the temperature rises. Also, it was observed that the total drain leakage current density $J_{TLeak}$ is given by the sum of electrons $J_{Electrons}$ and holes $J_{Holes}$, but according to the analysis, it was noticed that $I_{DLeak}$ is composed mainly by electrons, for all devices investigated.

6. REFERENCES


5. CONCLUSIONS

In this study it was verified the behavior of the drain leakage current $I_{DLeak}$ and its composition, in DGFinFET SOI nMOS devices operating since room temperature up to 300 °C.