DESIGN AND CHARACTERIZATION OF A 900MHZ LC VOLTAGE CONTROLLED CMOS OSCILLATOR

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ABSTRACT

This work presents the design and characterization of a 900MHz complementary cross-coupled LC voltage controlled oscillator (VCO). The circuit was prototyped in standard 0.35µm CMOS technology. It consumed 3.5mW with phase noise as low as -76.8dBc/Hz @100kHz in characterization. The VCO tuning range achieved 210MHz and an average gain of 87.5MHz/V.

1. INTRODUCTION

Some important characteristics of the transceivers such as channel resolution and bandwidth depend heavily on the performance of the oscillators used.

As the RF transceivers become more complex, higher data rates are demanded and system bandwidth and power must not grow, the design of better oscillators become a center problem [1].

The circuit prototyped in this work will be part of a 900MHz frequency synthesizer used in an RF transceiver of a system on chip for wireless sensor network. Such transceiver must work in ISM (industrial, scientific and medical) 900MHz with narrow channel bandwidth and consume low power.

In section 2, the VCO design will be described. Test results will be shown in section 3. Section 4 presents the conclusion of this work.

2. VCO DESIGN

In LC oscillators the frequency is strongly dependent on the inductor and capacitor values and weakly dependent on other variables such as transistor sizes, power or biasing. In the simplest model, the output frequency can be calculated as:

$$f_{out} = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

Therefore it is a common approach to control the oscillating frequency by varying the capacitance of the circuit once the inductance is fixed for a given inductor layout.

Integrated varactors can be implemented using reversed biased PN junctions [1] [2] or MOS capacitors [3]. Both strategies present good quality factors [1] making the output phase noise basically a function of the inductor's quality factor and consumed power.

In this work, reversed biased PN junctions were used because they lead to a more linear relationship between output frequency and control voltage and a wider control voltage range when compared with MOS capacitors.

A simplified schematic of the designed circuit is shown in Figure 1. It is a CMOS astable multivibrator and the LC tank selects the output frequency. The topology was chosen as a trade off between power consumption and phase noise. Oscillators with only NMOS transistors are able to achieve better noise characteristics if larger power is available[1]. The used complementary topology presents better phase noise when lower power is a center goal.

The MOS transistor sizes are shown below.

Table 1: MOS transistor sizes

MOS Transistors	W	L
M1 and M2	80µm	0.35µm
M3 and M4	240µm	0.35µm
M5	80µm	0.35µm
M6	40µm	0.35µm

The transistors M3 and M4 were sized to have the same transconductance of transistors M1 and M2 because that prevents noise upconvertion.

The inductors used presented 9.15nH and quality factor of 1.5 at 900MHz. They were available in a custom cell library and had already been characterized and modeled for this frequency.

The varactors were implemented using 26 emitter-base junction of vertical PNP bipolar transistors connected in parallel. The number of varactors used led the circuit to a wide tuning range. The control voltage is connected to the emitter of all the BJT.

The design strategy employed Cadence [4] Spectre RF tool to optimize the devices dimensions (according to the circuit specifications) through an iterative way.

The circuit in this work was prototyped in AMS[5] 0.35µm CMOS technology.

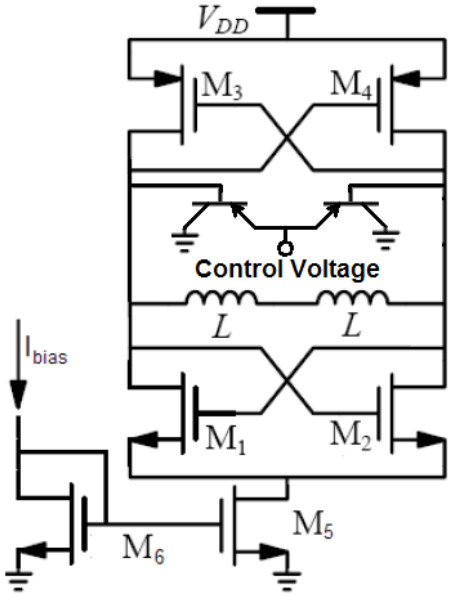

Figure 1: Simplified schematic of the prototyped circuit.

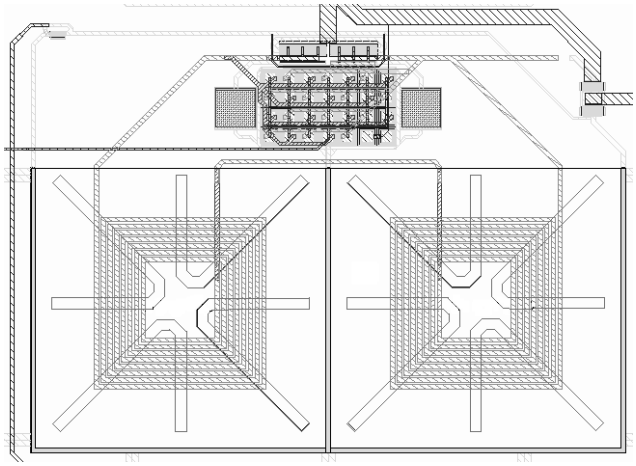

Figure 2: Layout of the prototyped circuit.

During design, the minimum power that could guarantee oscillation was 3.5mW. The power could be varied controlling the bias current in case better phase noise is demanded.

The tuning range was made wide to guarantee that the circuit would always work in the desired range despite all process variations. During fabrication the junction capacitances vary randomly in a tolerance band affecting the output frequency.

A maximum 2V tuning control voltage was chosen in order to maintain the PN junctions permanently reversed biased.

Figure 2 presents the circuit layout. This layout was drawn symmetrically in order to avoid noise upconvertion, reducing phase noise and consumed 0,24mm².

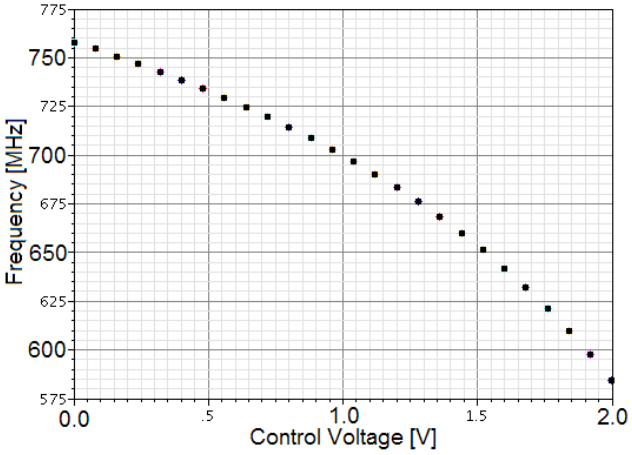

Figure 3: Relationship between control voltage and output frequency in post-layout simulation.

The post-layout simulations were made based on the layout presented taking into account parasitic

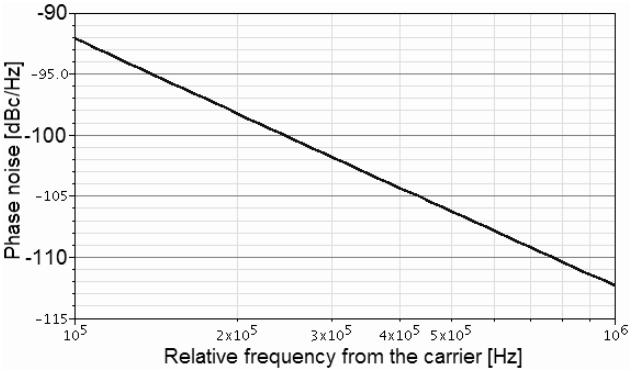

Figure 4: Post-layout simulated phase noise.

capacitances and resistances. As it can be seen in Figure 3 the parasitic capacitances lowered the output frequency. As a consequence of the parasitic resistances

the necessary power need to start oscillation in this simulation raised to 6.6mW. The phase noise characteristic in post-layout simulation is shown in Figure 4.

As it can be seen in Table 2, the circuit performance is comparable with other works.

Table 2: Comparison among works

Work	Technology	Frequency (GHz)	Power (mW)	Tuning range (%)	Phase noise (dBc/Hz)
[6]	0.7µm CMOS	1.8	6	14	-116 @600kHz
[7]	1µm CMOS	0.9	10.4	14	-95 @600kHz
[8]	0.25µm CMOS	1.8	6	0	-121 @600kHz
[9]	0.8µm BICMOS	0.4	1.7	38	-99.7 @100kHz
[10]	0.18µm CMOS	2.0	0.5	7	-111 @1MHz
This Work	0.35µm CMOS	0.75	6.6	23	-108 @600kHz

3. MEASUREMENT RESULTS

In Figure 5, a picture of the circuit during measurement is shown. A power consumption of 3.5mW was obtained in characterization. This result is better than expected in simulation with parasitics and shows that parasitics were overestimated in simulation.

Observing the overall characteristic the circuit works as desired.

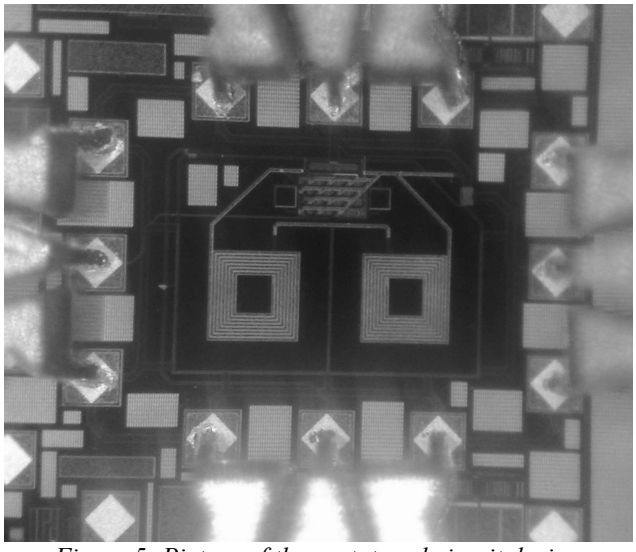

Figure 5: Picture of the prototyped circuit during measurement.

The spectrum of the generated signal can be seen in Figure 6.

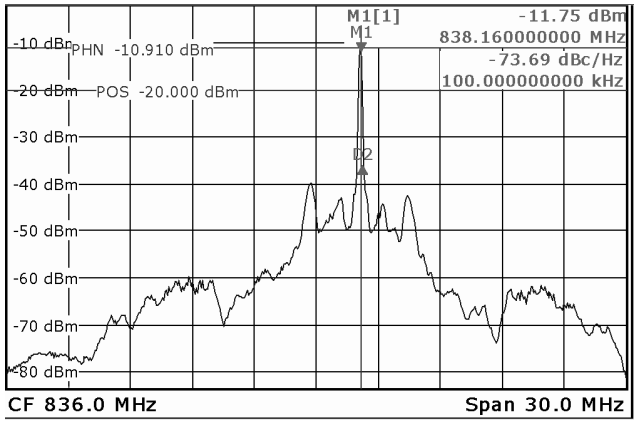

Figure 6: Spectrum of the measured signal.

Once the generated RF signal is large, approximately 300mV, the capacitance of the junctions is being changed by the RF signal. As the relationship between control voltage and junction capacitance is non-linear, intermodulation products are being added. The simulated phase noise was -92dBc/Hz @ 100kHz. The measured phase noise was -73.69dBc/Hz @ 100kHz. The intermodulation affected the phase noise measurement.

The measured relationship between output frequency and control voltage is shown in Figure 7. This Figure was obtained with default biasing voltage, 3.3V for the technology used.

Uncommon discontinuities in the relationship shown in Figure 7 are observed. The measurement resolution has been increased in the discontinuities regions in order to study it's behavior more accurately. It is observed that the discontinuities happen in a small control voltage variation such as 10mV. This effect is still being studied.

A good tuning range was also obtained. The circuit presented a 210MHz tuning range, 25% of the maximum frequency obtained. The VCO average gain is 87.5MHz/V.

As a form of adjusting the center frequency of the oscillator, one could vary the biasing voltage and current. This strategy must obey technology limits for voltages and current densities. The prototyped circuit reaches frequency specification for a 5V biasing voltage.

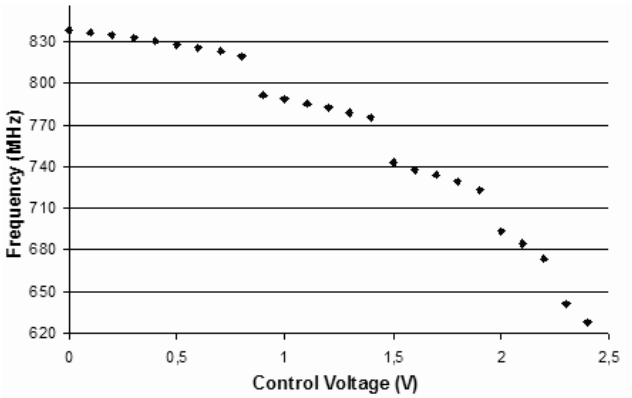

Figure 7: Measured relationship between output frequency and control voltage.

4. CONCLUSION

A differential cross-coupled complementary LC oscillator was designed, prototyped and characterized.

The circuit consumed 3.5mW and a 210MHz tuning range was observed.

The center frequency was lowered by parasitic capacitances but the circuit reaches specification with a change in bias condition.

A redesign taking into account the parasitics and further study on the discontinuities of the relationship between output frequency and control voltage shall be carried out.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

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