VHDL-AMS MODELING OF ANALOG/MIXED-SIGNAL IP BLOCKS

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ABSTRACT

This paper describes the modeling in VHDL-AMS of a voltage-to-current converter and an analog-to-digital converter, with the purpose of allowing high-level simulation of complex systems. The models describe actual devices, manufactured and currently being tested. Throughout the paper, they are used as case studies to show how modeling analog and mixed-signal (AMS) circuits in hardware description languages can be an important step in generating IP blocks.

Each of the models was simulated both isolated and as part of a system. Results of simulation reinforce the value of high-level modeling for integrating analog and mixed-signal IP.

1. INTRODUCTION

This paper presents the modeling of two analog/mixed-signal (AMS) circuit blocks in VHDL-AMS, motivated by the usefulness of high-level models both in simulating complex systems and in generating Intellectual Property (IP) blocks from AMS circuits. The development of this work is based on circuit blocks previously designed as part of a system-on-chip (SoC) for wireless networks with sensors. The SoC referred to here is dedicated to optimization of water management on crops, through irrigation control, and is further detailed in [1]. It includes, among other modules, an analog interface, that receives analog signals from the sensors, converts them into digital signals, and delivers them to a microprocessor.

The interface is partially composed of a current-mode analog-to-digital converter (ADC) and a voltage-to-current (V-I) converter. Both blocks have been validated and manufactured. Since a high-level description of the digital parts of the SoC (already validated and manufactured as well) have been developed, a high-level description of the analog and mixed-signal (AMS) portions was desired as well, thus allowing validation of the entire system and the generation of an heterogeneous virtual platform in which the software applications can be run and optimized in an early stage of the design.

The structure of this paper is as follows: in the Methodology section, the models development will be presented and justified, as well as implications of this work to further developments in mixed-signal systems, especially regarding AMS IP blocks. Then, section 3 (Case Study: Analog Interface) will present details of the AMS blocks and their VHDL-AMS models. Simulation results will be shown in section 4, Simulation and Discussion. Finally, in the Conclusion, a brief review is made of the methodology and results, in order to analyse current achievements and proposals for future work.

2. METHODOLOGY

For complex systems, high-level models are useful as they allow different functionalities to be assessed with relative ease. The SoC referred to here, for example, would require impeditive computational effort to be simulated entirely in transistor-level. The digital sections have already been modeled in SystemC for system-level behavioural description. It should be mentioned that, for the present work, modeling mixed-signal blocks with SystemC-AMS was put aside for the moment, mostly because AMS extensions for SystemC are still too recent – the language reference manual had its draft #1 released in december, 2008 [2]. Furthermore, if the co-simulation of different hardware/system description languages is achieved, then the methodology can be applied again later with few restrictions.

2.1. VHDL-AMS modeling

The different levels in the VHDL-AMS models are to be used each according to the accuracy and complexity desired in simulation. (The complexity required of different abstraction levels is discussed in several works, such as [3] - [5].) The work described here used predefined IEEE libraries for VHDL-AMS [6] to create the models of each block and a testbench, which generates stimuli, instantiates all entities and connects them together. The interfaces were described as electrical terminals. An external signal generator was also created, because in co-simulation with other systems the testbench is not included, only the circuit blocks. The models of both blocks were developed according to the following steps.

Firstly, the specifications of the block are translated into the ideal model, particularly regarding the interface. Not all ports included are necessary for the ideal model, but since VHDL-AMS allows for different *architectures* (descriptions) of the same *entity* (the functional block), they were kept to maintain cohesion throughout different levels. The ideal architecture models the block according to desired specifications only. Then, for lower-level models, non-ideal characteristics are described as well, preferably in a parameterised way. Examples of this are the tolerance to temperature and ouput range limitations of the V-I converter, and offset, gain error and integral and differential nonlinearities of the ADC. Internal

structure and circuitry is described only in the lowest level.

After the validation of the model, simulation results are compared both to the original block's specifications and to its electrical behaviour – so far, only results extracted from BSIM3V3 simulations, since both blocks were prototyped but are currently still being tested. Measurement results, when ready, will be incorporated to the lowest level model. Parameterisation makes this process much easier.

2.2. IP description

IP blocks are essentially previously designed and validated circuit blocks which can be integrated into different systems, saving design time for the purchaser. Currently, analog IP blocks are delivered mostly as *hard* IP – optimized, technology-specific physical layouts, usually delivered as a GDSII file and a set of documentation [7]. The main advantage of such approach is that the design can be greatly optimized before delivery. Its greatest disadvantage is the lack of flexibility to the design. Digital IP blocks, on the other hand, are usually provided as synthesizable RTL codes (*soft* IP), which allows for greater flexibility, but at the same time compromises the protection of the developer's intellectual property.

The possibility of simulating HDL designs of whole functional blocks, even along with electrical schematics, points to the use of high-level models as part of the set of deliverables of an IP block. This was referred to by VSIA [8] and, later, by Freescale's Semiconductor Reuse Standard [7], although only a high-level behavioural model was recommended. With the development of analog and mixed-signal HDL extensions and even improvement of automated analog synthesis [9], high-level models of AMS circuits show an increasing importance.

For the purchaser to assess whether a given IP block (or *virtual component*, VC) is suitable for his application or system, the block's specifications are usually a sufficient means. However, a black-box model that can be easily simulated as part of different systems is an invaluable tool. It allows purchasers to choose which (if any) VC is most useful for their purposes, and can be delivered by the provider without worries regarding intellectual property protection.

Complex technology-specific files might not be needed in the initial stages of a project, when a high-level model would be more than sufficient – as long as the model behaviour is accurate. A single parameterized model can even describe several different hard IP blocks, with minor choices during simulation.

3. CASE STUDY: ANALOG INTERFACE

The analog interface in the SoC acquires analog data from external sensors, performs the necessary conditioning, converts the signals to strings of binary digits, and delivers the bits to the microprocessor. The two main mixed-signal blocks in the interface, the V-I converter and the ADC, also receive instructions from the processor: the V-I converter, though almost entirely analog, can be switched to normal operation, off, or to test mode, by digital signals; the ADC receives and delivers several different digital instructions, notably a clock signal, an on/off signal, and control bits used to inform the processor of the ADC's operation.

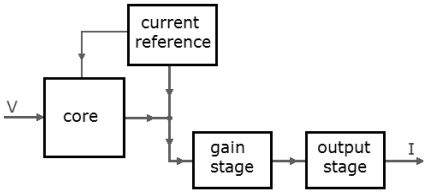

Figure 1 – V-I converter diagram

Next, some description of the specifications of the converters is given, presenting only the details that are relevant to the present discussion.

3.1. Voltage-to-current converter

The V-I converter is composed by four different circuit blocks – a current reference, a conversion core block, a gain stage and an output stage (Figure 1). The input voltage ranges between 1.0 V and 2.0 V; after internal processing, its current output ranges between -100 µA and +100 µA, linearly correspondent to the voltage input. Three switches can allow access to internal nodes, cut off the input and output, and reduce power consumption. Further details on topology and operation can be found in [10] and [11].

The VHDL-AMS ideal model of the V-I converter simply implements the control switches and the relation between the block's input voltage (*VI_V_IN*) and output (*VI_I_OUT*). In lower abstraction levels, the model takes into account non-ideal effects, such as a difference that appears in the output/input relation for the positive and negative output range, and the influence of the temperature in the circuit's behaviour.

ideal behaviour

```
IF vi_d_cin = '1' USE
      vi_i_out == (vi_v_in-1.5)*2.0e-4;
ELSE
      vi_i_out == 0.0;
END USE;
break on vi_d_cin;
```

non-ideal behaviour

```
constant coef_t00_27 : real := (195.32 + (27.0 - temp_c)/1.697)*1e-06;
constant coef_t27_70 : real := 9195.32 + (27.0 - temp_c)/1.915)*1e-06;
...
IF vi_d_cin = '1' USE
      IF temp_c > 27.0 USE
            vi_i_out == (vi_v_in - 0.95189)*coef_t27_70 - 106.827e-06;
      ELSE
            vi_i_out == (vi_v_in - 0.86801)*coef_t00_27 - 123.210e-06;
      END USE;
END USE;
break on vi_d_cin;
```

Figure 2 – VHDL-AMS partial code for V-I converter

A comparison between a few statements in the ideal model and a lower-level model is shown in Figure 2,

where the temperature's influence is parameterised by the factor `temp_c`, through the use of equations obtained from electrical simulations. The `break` statements in the non-ideal model tell the analog solver that the model's state has to be re-evaluated if the digital control signal is resetted.

3.2. Analog-to-digital converter

The analog-to-digital converter works with a sampling rate of 50 ksps. It samples the input current, within a range of -100 µA to 100 µA, at the beginning of each conversion cycle, performs a series of comparisons between the sampled input and a reference, and delivers a string of 8 bits at the eight last clock rising edges of the cycle, starting with the least significant bit (LSB). Digital signals received from the microprocessor include an on/off switch and a 16 MHz clock signal.

In a high level of abstraction, the VHDL-AMS block *ad_ideal* models the behaviour of the ADC. Simultaneous statements model its underlying electrical behaviour, while sequential statements model the logical operation. The timing of the conversion is controlled by the clock digital signal, but for most of the conversion cycle the block is idle; this is done to consider the time needed for the conversion cycle, in the physical design.

The actual design for the ADC includes several control signals, mostly concerning test structures, but for a high-level behavioral description they can be ignored. More details on the ADC can be found in [12] and [13].

As mentioned, the manufactured block is still under test, so actual limitations still have to be described. However, the VHDL-AMS lower-level model *ad_comp* includes various non-ideal effects characteristic to ADCs, such as offset, gain error, integral nonlinearity (INL) and differential nonlinearity (DNL). These appear in the model (as shown in Figure 3) as *generic* ports (not being actual input signals), parameterised to facilitate feedback from prototype measurements.

The model *ad_comp* was built in a way that a value of zero for all effects means it behaves ideally. Modeling these effects separately is a bit tricky, since an isolated quantitative analysis of one effect can hide another; so superimposing independent measures can lead to distortions. Besides, the INL and DNL are usually defined by their maximum value [14], and this gives no information on where, in the input/output characteristic, they occur. So the designer has to gather information directly from tests, to ensure the model will be acurate.

```
entity ad_comp is
     generic ( ad_offset : real := 0.0e-06;
               ad_gerr : real := 0.0;
               ad_INL : integer := 0;
               ad_DNL_in : bit_vector ;
                     ad_DNL_out : bit_vector ;

     port (  terminal  AD_A_INPUT : electrical;
             signal  AD_D_RD_Out_Byte : out bit;
             signal AD_D_CLK : in bit;
             signal AD_D_ON_OFF : in bit;
end entity ad_comp;
```

Figure 3 – VHDL-AMS entity declaration for the A/D

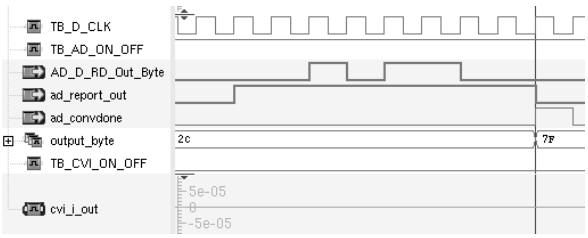

Figure 4 – simulation of the interface model

4. SIMULATION AND DISCUSSION

The VHDL-AMS models designed have been simulated using Cadence Design Systems' NCSim feature. In Figure 4, it can be seen a portion of the resulting waveforms from a simulation of both high-level blocks connected together. It can be noticed that the ADC model's internal variable *output_byte*, which stores the result from conversion changes when the last output bit is delivered. This is because in the VHDL-AMS simulation, there is no delay in calculation, so at the same moment that the input is sampled, the result is available internally.

Figure 5 show, to the left, an overlay of two waveforms resulting from simulation of the V-I converter's model, for a 22 kHz senoidal input voltage signal. The outer, darker wave represents the ideal current output; the inner, lighter wave represents the intermediate-level model output, mentioned in the previous section. These results are in accordance to the actual measured design of the V-I converter [10], as can be seen in the right-hand half of Figure 5, which shows current waveforms from ideal and non-ideal electrical simulations.

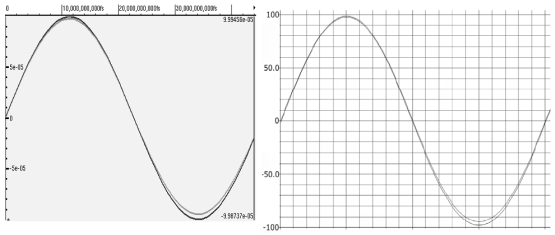

Figure 5 – VHDL-AMS and electrical simulations

The non-ideal effects of the ADC were simulated in operation as well, although, to plot the results as input versus output, the modeled behaviour was translated into a MatLab algorithm. Figure 6 shows the resulting graphics for (a) offset, (b) gain error, (c) INL and (d) DNL. Arbitrary values were used, just to demonstrate the difference between ideal and non-ideal characteristics.

5. CONCLUSION

This work has presented the successful development of high-level models of real, manufactured analog and mixed-signal circuit blocks. They were modeled in VHDL-AMS, and used in the present work as an example for a broader methodology useful in the context of AMS

IP blocks: if high-level models are incorporated into the set of files provided as part of an IP, potential purchasers can beforehand analyse the utility of the block in their systems with great flexibility, without risk to intellectual property protection. Therefore, models in HDL of AMS circuits are useful even if analog synthesis is not available.

An underlying limitation of this method is, of course, that the more accurate is the model, the more complex it will be, thus taking more time to develop and requiring more computational effort. Future work includes a SystemC/VHDL-AMS co-simulation of the complete SoC for software development and optimization, and incorporating the results from prototype measurements into the models. The same blocks will also be modeled in Verilog-AMS and SystemC-AMS, in different abstraction levels, in order to assess advantages and limitations of each language and to perform different analyses, such as system performance. These blocks will also serve as part of an actual analog IP block, validating the proposed course of action.

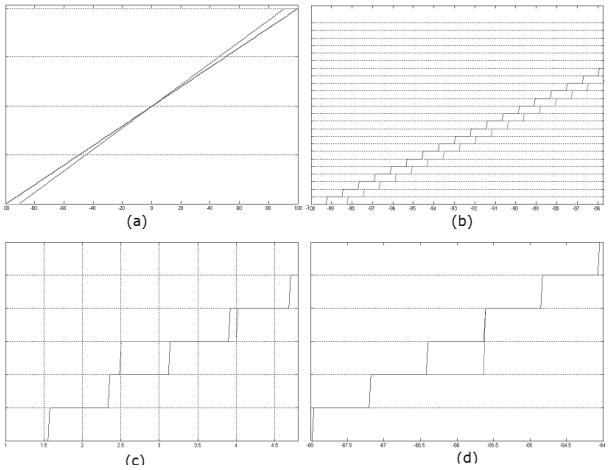

Figure 6 – ADC non-ideal effects

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7. ACKNOWLEDGEMENTS

The authors would like to thank CNPq (Brazilian government agency) for financial support.