ON THE ELMORE "FIDELITY" UNDER NANOSCALE TECHNOLOGIES

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ABSTRACT

In the middle of the nineties, it have been stated that, despite some issues regarding the Accuracy Property of the Elmore Delay Model [1], the Fidelity Property of it, makes this model capable of properly ranking routing solutions, thus, allowing an efficient comparison between different Interconnect Design approaches, methodologies or algorithms. In this work, we dive more deeply on the Fidelity Property of Elmore Delay, by analyzing it under nanoscale interconnect parameters, showing how does it behaves while scaling down to 13nm processes. We notice a high standard deviation in the Fidelity analysis, what invalidate such criterion as a confident metric for comparisons.

1. INTRODUCTION

The Elmore Delay Model (EDM) is well known as an analytical model for interconnect delay. Efficient and ease to use, it is also known the inaccurate estimates it provides in some spots of the target interconnect structure, specially in the parts close to the source (or driver). Despite of this inaccuracy that it presents sometimes (due to an overestimated downstream capacitance, that is actually diminished by the resistive shield), it have been verified that the EDM provides a considerable *Fidelity* when ranking routing solutions. That means, once different routing solutions are given to a given routing problem, it provides a similar, or even the same, rank as electrical simulation, thus, allowing to evaluate and compare different routing techniques, then picking the best one with a fine degree of certainty. That was called the "*Fidelity* Property" of the EDM. This property represented a good reason for using EDM in Interconnect Design research. Even knowing that the model was not accurate enough for many applications, since the early nineties [2] [3] [4] [5] until recently [6] [7] [8] [9] it has been used as a metric for routing algorithms evaluation and comparison.

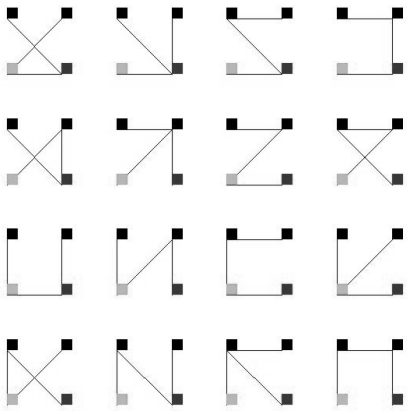

Figure 1. The spanning trees for a 4-pin net.

In section two we reproduce the experiments of [2]. In section three we define more realistic and up-to-date scenarios for the new experiments, based on nowadays technologies and different grid sizes according to the scope of routing (local/detailed, long/global, system-level). In section four we describe the experimental results, followed by the conclusions and future work.

2. REPRODUCTION OF THE PREVIOUS EXPERIMENTS

The Fidelity Property was defined based on a standard rank-ordering technique used in the social sciences [10]. In [2] they used the rank-ordering technique of [10] to analyze the Fidelity of the ranks provided by EDM for the whole set of possible spanning trees of randomly generated point sets (or nets), in respect to SPICE simulation ranks. Based on the comparison of the average of the absolute difference between both ranks, they assumed that EDM provided high Fidelity delay criterion. First, for reproducing the experiments, we had to consider the whole set of possible spanning trees for each one of the nets. Two sets of 50 randomly generated nets, one for each net size: 4 and 5. For nets with 4 terminals there are 16 possible solutions – Figure 1 – and for nets of 5 terminals there are 125 ($|N|^{|N|-2}$).

The set of solution for each net is ranked both by Elmore and *hspice* delay results. Table 1 then shows the results with the difference between both ranks, given for the best case, five best cases, and the average differences for the whole 50 nets of each net size. They are both the results for a given randomly-chosen critical sink in each net, and the worst delay for each net as well. Those results were obtained with the interconnect parameters provided in [2], for three different processes: 2.0µm, 1.2µm, and 0.5µm. It is not clear in [2] the area that was considered for generating the random point sets, except for saying that the random nets had "*pin locations chosen from a uniform distribution over the routing area*", though they provide the typical die size of 1cm^2 for these processes. So, we tried to enclose the actual grid size by using the total die size area, and a small size area of 500x500µm. Thus, there are three columns underneath each net size in Table 1, those are respectively, the original values from [2], the values achieved by

Table 1. Average difference between Elmore and hspice delay rankings. Comparison of the results from [2] with our experiments on both a 1cm² and a 500x500um grids. The rank position differences for a critical sink delay and for the worst sink delay in three cases: best case, 5 best cases, and the average of the routing solutions for each net in each net size.

	Tech.	Case	Net size = 4			Net size = 5		
			[2]	1 cm²	0.25mm²	[2]	1 cm²	0.25mm²
CRITICAL SINK DELAY	2.0µm	Best	0.54	0.00	0.00	5.90	0.09	0.05
		5 Best	1.02	0.21	0.10	7.20	0.38	0.15
		All	0.92	0.31	0.14	8.00	2.70	1.58
	1.2µm	Best	0.58	0.63	0.00	6.40	5.34	0.05
		5 Best	0.99	1.08	0.19	7.20	5.91	0.33
		All	0.94	0.88	0.30	7.90	7.90	2.73
	0.5µm	Best	0.58	0.58	0.58	5.60	5.81	6.08
		5 Best	0.93	1.08	1.07	6.50	6.01	6.42
		All	0.93	0.84	0.88	7.70	7.88	8.02
	Tech.	*Case*	Net size = 4			Net size = 5		
			[2]	1 cm²	0.25mm²	[2]	1 cm²	0.25mm²
MAXIMUM DELAY	2.0µm	Best	0.38	0.00	0.00	0.10	0.09	0.05
		5 Best	0.71	0.01	0.00	0.47	0.28	0.14
		All	0.65	0.09	0.10	1.39	1.97	1.19
	1.2µm	Best	0.16	0.10	0.05	0.20	0.16	0.09
		5 Best	0.51	0.20	0.05	0.53	0.89	0.26
		All	0.43	0.24	0.11	1.24	3.88	1.87
	0.5µm	Best	0.48	0.00	0.00	0.20	0.44	0.48
		5 Best	0.52	0.07	0.15	0.44	1.04	1.05
		All	0.60	0.15	0.20	1.22	3.98	3.99

reproducing their experiments with the large grid of 1cm², and, finally, the values achieved with the small grid. Closer values were achieved with the 1cm² grid, suggesting that the original grid was closer to this one rather the 500x500µm one.

Further, in the work of [2] it is not very clear whether a given Fidelity value is much of few better than another one. On an attempt to justify that Elmore delay had a high Fidelity for the critical-sink delay criterion, (and nearly perfect Fidelity for the maximum sink delay criterion) they exemplified that, with the 5-pin nets and the 0.5um technology, optimal critical-sink topologies under Elmore delay averaged only 5.6 rank positions (out of 125) away from optimal according to SPICE, while the best topology for maxi-mum Elmore delay averaged only 0.2 positions away from its "pro-per" rank using SPICE. In our case, we can find the values 5.81 and 0.44, respectively for the same cases.

3. DEFINITION OF THE NANOSCALE INTERCONNECT SCENARIOS

We are going to use technological RC parameters related to technologies with channel lengths ranging from 350nm down to 13nm from [11]. Those are based on the interconnects classification of the International Technology Roadmap for Semiconductors [12] providing different parameters for *metal 1*, *intermediate* and *global* wires, according to the metal layers. In [11], for each technology there are three parameter sets defined accordantly to the ITRS classification. We make use the sets for intermediate and global wires, since those comprise local and global networks, respectively.

Also, it became evident from the experiments of the previous section that the grid size provides significant impact on the results obtained. Thus, we are going to consider different grid sizes according to the type of routing (and related metal levels). First we will use 200mm² as a reasonable SoC die area, based on an average of some die area values available at [13], comprising Intel and AMD processors. As observed in [14], the long global connections of the SoC designs will

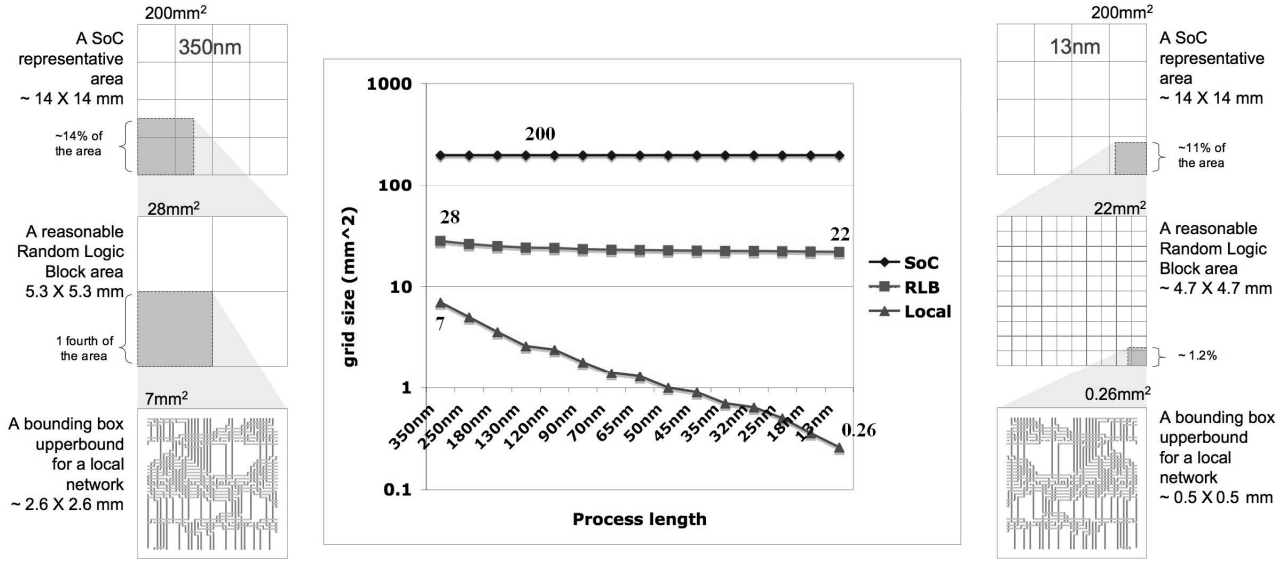

Figure 2. Grid Sizes for each technology (center). On the left, for 350nm, the grids for SoC, RLB and Local networks, and on the right respectively the grids for 13nm.

Table 2. Interconnect scenarios for the experiments.

	Routing Grids		
Metal Layers	Local	RLB	SoC
Intermediate	Scenario 1	Scenario 2	-
Long Global	-	Scenario 3	Scenario 4

not scale in length as much as the local interconnects related to detailed routing. Therefore, we defined the same 200mm^2 "SoC grid" for all technologies, since this parameter do not present the same decreasing as smaller grids due to integration increase. We then define 14% of this area as a typical area for a random logic block (RLB) in a 350nm technology. A fourth part of the RLB area was then defined as a fine upperbound for local networks inside a RLB. After that, we extrapolate the local routing grid to the smaller technologies in respect to the 350nm. The relation between the RLB grid and the other ones is also used for defining the other technologies' grid sizes, resulting in the grid sizes plotted in the chart of Figure 2.

We then define the four interconnect scenarios of Table 2, based on the Interconnect parameters and routing grids previously considered.

4. EXPERIMENTAL RESULTS

Now, considering the four interconnect scenarios of Table 2, we evaluate the Fidelity Property of EDM. From Table 3 to Table 6 the results for each one of the four interconnect scenarios of Table 2 are respectively shown, for the 15 technologies ranging from 350nm to 13nm. The tables are similar to Table 1, except that we provide standard deviation for the cases *All* and *5 Best*. For the case *Best* we provide the maximum ranking difference found, specified as "> diff" in the corresponding column. Due to space limitations we are showing only the results for the randomly chosen critical sink, because that is where the average differences are more pronounced.

Considering the average difference for the whole set of solutions for each net (case *all*) a huge standard deviation is present in the experimental results. This standard deviation is always larger than the corresponding average. In the case of considering the *5 Best* delay topologies for each net, the standard deviation is smaller, although still considerably large, around half of the corresponding average in general. For the three cases, the delay criteria are still similar to the previous experiments of section 2. It is noticeable that, along technological scaling, the fidelity is slightly improved, however, we can see that the maximum ranking difference found for the case *best* in 5-pin nets, ranges from 15 to 26 rank positions for the smaller technologies in all scenarios. The maximum position differences found in the overall experiments are: 8 for 4-pin nets and 84 for 5-pin nets.

Though one can say that, in performance driven routing the cases *best* and *5 best*, which present a smaller standard deviation than case *all*, are the ones of interest, since those comprise the routing topologies of smaller delays, the standard deviation provided by them is still considerably large. In the chart of Figure 3 we summarize some results for maximum sink delay. We plot the results for *5 Best* case both in interconnect scenario number 1 and scenario number 4, for 4-pin nets. We can see how the standard deviation is always larger than the average values, and also, how scenario 4 used to provide the worst results forthe larger length

Table 3. Results for scenario number 1.

	Net size = 4						Net size = 5					
Case:	Best		5 Best		All		Best		5 Best		All	
Tech.	AVG	>diff	AVG	S.D.	AVG	S.D.	AVG	>diff	AVG	S.D.	AVG	S.D.
13nm	0.47	5	0.97	0.59	0.83	0.99	5.05	25	6.81	3.53	8.01	8.33
18nm	0.51	5	0.94	0.59	0.81	1.00	5.10	26	6.69	3.31	8.02	8.37
25nm	0.47	5	0.98	0.60	0.82	1.01	5.05	25	6.80	3.56	8.02	8.36
32nm	0.47	5	0.91	0.58	0.81	1.01	4.76	25	6.56	3.42	7.96	8.28
35nm	0.40	5	0.91	0.57	0.80	0.97	4.52	24	6.54	3.45	7.91	8.24
45nm	0.21	4	0.86	0.62	0.74	0.92	3.72	21	5.55	3.17	7.69	8.01
50nm	0.21	4	0.88	0.66	0.72	0.92	3.42	21	5.07	2.87	7.59	7.90
65nm	0.13	5	0.61	0.54	0.59	0.80	2.00	17	4.01	2.15	7.01	7.44
70nm	0.32	5	0.60	0.49	0.59	0.79	2.07	15	3.46	1.88	6.73	7.21
90nm	0.19	2	0.43	0.41	0.51	0.70	1.01	8	1.78	1.34	5.38	5.85
120nm	0.00	1	0.27	0.33	0.38	0.59	0.43	6	0.69	0.56	3.71	4.03
130nm	0.00	1	0.22	0.29	0.34	0.49	0.27	3	0.59	0.44	3.31	3.54
180nm	0.00	0	0.18	0.23	0.25	0.41	0.08	1	0.33	0.28	2.70	2.71
250nm	0.00	0	0.21	0.27	0.30	0.42	0.04	1	0.35	0.37	2.75	2.84
350nm	0.00	1	0.24	0.29	0.35	0.54	0.39	6	0.63	0.51	3.51	3.76

Table 4. Results for scenario number 2.

	Net size = 4						Net size = 5					
Case:	Best		5 Best		All		Best		5 Best		All	
Tech.	AVG	>diff	AVG	S.D.	AVG	S.D.	AVG	>diff	AVG	S.D.	AVG	S.D.
13nm	0.62	2	0.87	0.75	0.83	0.96	5.30	18	5.13	3.32	7.10	8.18
18nm	0.62	2	0.86	0.72	0.84	0.96	5.36	18	5.23	3.27	7.16	8.20
25nm	0.58	3	0.88	0.74	0.84	0.98	5.63	18	5.42	3.40	7.28	8.28
32nm	0.62	4	0.91	0.75	0.85	0.98	5.78	18	5.56	3.46	7.38	8.38
35nm	0.54	4	0.89	0.70	0.85	0.97	5.74	18	5.67	3.58	7.44	8.43
45nm	0.62	4	0.96	0.75	0.86	0.98	5.74	18	5.77	3.57	7.58	8.47
50nm	0.58	4	1.02	0.79	0.86	1.00	6.09	26	6.04	3.33	7.68	8.49
65nm	0.55	4	1.04	0.71	0.89	1.01	6.28	25	6.42	3.45	7.90	8.54
70nm	0.55	4	1.06	0.69	0.91	1.02	6.20	28	6.53	3.51	7.95	8.51
90nm	0.58	5	1.04	0.66	0.88	1.02	5.96	26	6.74	3.35	8.07	8.42
120nm	0.21	4	0.83	0.61	0.74	0.93	3.10	21	5.01	2.66	7.47	7.81
130nm	0.21	5	0.69	0.55	0.64	0.82	2.08	17	4.14	2.23	7.08	7.53
180nm	0.19	2	0.44	0.37	0.51	0.67	0.90	8	1.64	1.29	5.28	5.75
250nm	0.08	1	0.41	0.38	0.47	0.66	0.74	7	1.25	1.11	4.88	5.29
350nm	0.31	2	0.50	0.42	0.53	0.71	1.06	8	2.12	1.45	5.71	6.22

Table 5. Results for scenario number 3.

	Net size = 4						Net size = 5					
Case:	Best		5 Best		All		Best		5 Best		All	
Tech.	AVG	>diff	AVG	S.D.	AVG	S.D.	AVG	>diff	AVG	S.D.	AVG	S.D.
13nm	0.77	2	0.96	0.77	0.86	0.98	5.58	18	5.30	3.32	7.08	8.18
18nm	0.77	2	0.95	0.77	0.85	0.98	5.66	18	5.36	3.36	7.12	8.21
25nm	0.73	2	0.93	0.76	0.85	0.98	5.74	18	5.53	3.29	7.18	8.23
32nm	0.73	2	0.95	0.78	0.87	0.98	5.78	18	5.65	3.34	7.24	8.28
35nm	0.73	3	0.94	0.78	0.87	0.98	5.77	18	5.66	3.40	7.25	8.30
45nm	0.73	4	0.94	0.77	0.85	0.98	6.00	18	5.79	3.48	7.34	8.35
50nm	0.77	4	0.95	0.77	0.86	0.99	6.16	18	5.80	3.48	7.36	8.38
65nm	0.77	4	0.98	0.78	0.87	0.99	6.19	18	5.93	3.70	7.46	8.48
70nm	0.77	4	1.00	0.76	0.88	0.98	6.23	18	5.89	3.69	7.50	8.51
90nm	0.77	4	1.02	0.75	0.86	0.98	6.42	18	6.19	3.73	7.63	8.55
120nm	0.74	4	1.17	0.80	0.91	1.06	6.69	26	6.68	3.32	7.87	8.63
130nm	0.70	4	1.09	0.74	0.88	1.04	6.65	26	6.67	3.35	7.91	8.66
180nm	0.73	4	1.16	0.74	0.97	1.10	7.26	27	7.17	3.67	8.19	8.84
250nm	0.77	5	1.09	0.71	0.97	1.12	7.67	28	7.91	3.48	8.35	8.91
350nm	1.07	5	1.32	0.73	1.08	1.17	9.43	28	8.45	3.79	8.65	9.29

Table 6. Results for scenario number 4.

	Net size = 4						Net size = 5					
Case:	Best		5 Best		All		Best		5 Best		All	
Tech.	AVG	>diff	AVG	S.D.	AVG	S.D.	AVG	>diff	AVG	S.D.	AVG	S.D.
13nm	0.77	2	0.80	0.70	0.76	0.90	5.60	15	5.34	2.99	6.83	7.86
18nm	0.77	2	0.80	0.70	0.76	0.90	5.49	15	5.33	3.08	6.84	7.88
25nm	0.77	2	0.81	0.71	0.76	0.90	5.53	15	5.40	3.12	6.86	7.90
32nm	0.77	2	0.81	0.71	0.76	0.90	5.53	15	5.46	3.16	6.88	7.92
35nm	0.77	2	0.81	0.71	0.76	0.90	5.54	15	5.45	3.16	6.89	7.93
45nm	0.77	2	0.85	0.72	0.78	0.91	5.54	15	5.50	3.19	6.91	7.96
50nm	0.77	2	0.86	0.74	0.79	0.92	5.54	15	5.49	3.19	6.94	8.00
65nm	0.77	2	0.87	0.75	0.80	0.93	5.62	15	5.48	3.22	6.97	8.04
70nm	0.77	2	0.87	0.75	0.79	0.93	5.61	15	5.49	3.27	6.98	8.06
90nm	0.84	2	0.93	0.76	0.82	0.95	5.62	15	5.52	3.25	7.05	8.16
120nm	0.73	2	0.94	0.77	0.86	0.98	5.78	18	5.56	3.30	7.19	8.24
130nm	0.73	3	0.94	0.77	0.87	0.98	5.77	18	5.62	3.47	7.24	8.30
180nm	0.77	4	1.00	0.76	0.86	0.98	6.79	18	6.20	3.70	7.53	8.54
250nm	0.88	4	1.08	0.79	0.88	1.01	7.49	19	6.75	3.81	7.80	8.67
350nm	0.89	4	1.15	0.86	0.92	1.02	8.37	23	7.31	3.90	7.96	8.85

technologies, and starts to present smaller differences between 90nm and 70nm, in contrast to scenario 1.

In the chart of Figure 4 we plot other results for maximum sink delay. This time comprising the results for *5 Best* case both in interconnect scenario number 2 and scenario number 3, for 5-pin nets. Those comprise the RLB grid, showing in a same grid a better fidelity when intermediate/semi-global interconnect parameters of old technologies are used.

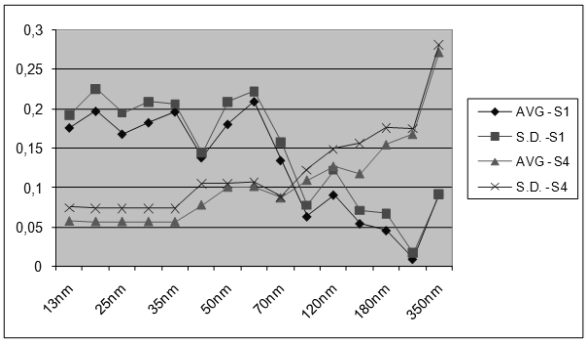

Figure 3. Results for maximum sink delay in 4-pin nets: average difference for scenario 1 (AVG-S1) and 4 (AVG-S4), and standard deviation for the same scenarios (S.D.- S1 and S.D.- S4, respectively).

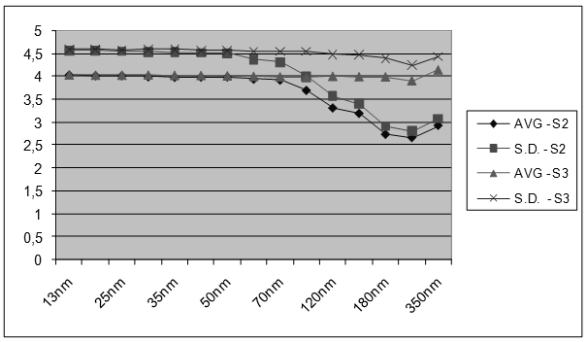

Figure 4. Results for maximum sink delay in 5-pin nets with RLB grid: average difference for scenario 2 (AVG-S2) and 3 (AVG-S3), and standard deviation for the same scenarios (S.D.-S2 and S.D.-S3, respectively).

5. CONCLUSIONS

We evaluated the Elmore Delay Model Fidelity property under robust nanoscale interconnect scenarios. Though the fidelity property previously established seems to slightly improve along scaling, the experimental results presented a significant standard deviation, showing that it is no longer a confident metric for routing techniques comparison inside the CAD/EDA research fields related to Interconnects.

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