

CROSS-SECTION SHAPE INFLUENCE ON SURROUNDING MuGFETs

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ABSTRACT

This work presents a study of the cross-section shape impact on surrounding multiple-gate FETs (MuGFETs) performance. Bearing this objective in mind, the results discussion was based on the analysis of very important parameters, such as the subthreshold slope and the threshold voltage, as a function of the transistors physical features for different cross-section shapes. After confirming the reliability of the simulation procedure by verifying the already know comparison between double-gate and quadruple-gate devices behavior, square, octagonal and circular channel section of surrounding gate transistors were highlighted. Therefore, by plotting the extracted subthreshold slope data, it was possible to conclude that the channel current control by the gate increased as the number of sides of the cross-section shape raises. The best results were obtained by circular surrounding gate transistor.

1. INTRODUCTION

The amazing CMOS integrated circuits development, which began with the advent of MOS transistors during the early 1960s, has been based on the continuous decrease in the physical dimensions in order to meet the performance expectations. This idea is deeply discussed in the world-famous “Moore’s Law” [1], according to which the number of transistors in integrated circuits uses to double every 18 months.

With this clear objective of keeping this MOS technology evolution, alternative technologies to the conventional one have been studied and, fortunately, some of them have presented quite interesting results, such as the Silicon-on-Insulator (SOI) one. Characterized by the presence of an insulator layer, often composed by SiO₂, between the silicon substrate and the transistor active region, SOI devices have been increasingly used during the last decade, mainly due to their applicability in harsh environments, in which low sensitivity to temperature variation and high hardness against transient radiation effects are required [2]. Besides, this structure avoids the undesirable short channel effect, allowing the project of transistors with reduced dimensions.

In spite of the SOI transistors longer life duration, the issue of the charges control in the channel region is still

considered a problem, particularly for channel length dimension lower than 100 nm, so that it is being exhaustively studied by the whole scientific community. In order to keep the continuous decrease in the MOS transistors dimensions in a way that they can reach 22 nm or less, the academic community is studying the applicability of a multiple gate structure. The multiple gate architecture has presented a better behavior when compared to the single gate one [3]. Among many observed advantages, it is possible to mention an increase in the transconductance, a decrease of the short channel effect and a better subthreshold slope.

The first double gate transistors were fabricated in the late 1980s, making use of SOI substrates and a similar fabrication process. Following the natural conceptual evolution, triple-gate SOI MOSFETs and triple-plus gate devices, namely Π -gate and Ω -gate transistors, have also been studied. Considering all this development, the structure that tends to present the best control of the channel region by the gate is the surrounding-gate MOSFET [4], traditionally projected with circular or square section shape.

Taking all this technological evolution into consideration, the goal of this work is to study the cross-section shape influence on surrounding-gate devices performance, focusing on short channel effects. In other words, this work has the aim of studying how the multiple-gate devices technological suitability may be maximized by the optimized geometrical project in terms of cross-section shape.

2. DEVICES CHARACTERISTICS AND SIMULATORS

The MOSFET transistors that are studied during this work present silicon film thickness (t_{Si}) of 20 nm and gate oxide thickness (t_{ox}) varying from 2 to 12 nm. The channel length (L) ranges from 10 to 100 nm.

In order to investigate the cross-section shape influence, devices with square, octagonal and circular channel sections were highlighted. Besides, these multiple-gate structures were compared to the double-gate one, so that the advantages of those more complex structures were confirmed. All the cross-section structures are exhibited in figure 1.

Finally, with the purpose of performing the numerical simulations, “Atlas 3D Devices Simulator” from Silvaco was used.

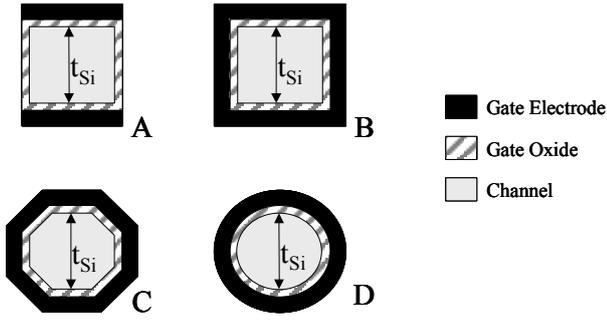


Figure 1: Simulated transistors cross-section view: double gate (a) and surrounding gate with square (b), octagonal (c) and circular (d) cross-sections.

3. METHODOLOGY

First of all, it is important to emphasize that all the comparisons of the different devices performance will focus on short channel effects mainly on two very representative parameters, namely the subthreshold slope (S) and the threshold voltage (V_{th}). These parameters were extracted based on the curves of the drain current as a function of the gate voltage ($I_D \times V_{GS}$), with drain voltage (V_{DS}) of 50 mV. The subthreshold voltage was extracted from the curve of the inverse of the logarithmic $I_D \times V_{GS}$ curve derivative; meanwhile, the threshold voltage extraction followed the linear extrapolation method, as it is shown in [5].

During the first part of this work, surrounding-gate devices with different cross-section shapes (square, octagonal, circular) were compared with each other and with double-gate transistors, considering the gate oxide thickness of 2 nm for all devices. The potential distribution was also analyzed.

The second part of the work focused on the performance dependence on the variation of the gate oxide and silicon film thickness ratio, in order to enable a quite comprehensive view towards this effect.

Finally, based on the obtained results, it was possible to compare the applicability of multiple-gate devices with different cross-section shapes.

4. RESULTS AND DISCUSSION

4.1. Comparison between double-gate and three different surrounding-gate devices

As it was previously explained, the first important group of results that will be presented is related to the comparison of three different kinds of surrounding-gate devices (square, octagonal, circular cross-section) and double-gate transistors.

The curves of subthreshold slope as a function of the channel length (S x L) are shown in figure 2.

At a first glance, it is possible to verify that the double-gate device presented the worst subthreshold slope behavior, exactly how it is already known by specific literature [4], confirming, therefore, the reliability of the simulated data.

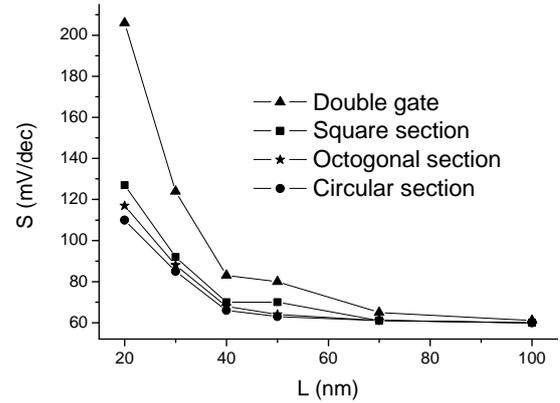


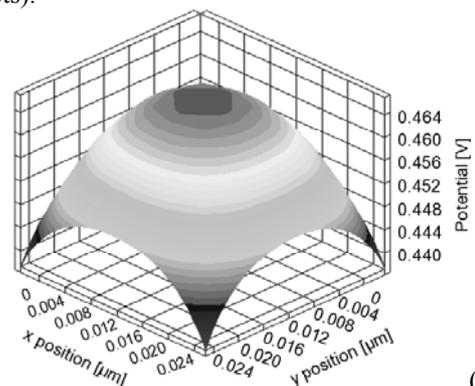
Figure 2 – Subthreshold slope (S) as a function of the channel length (L) for transistors with different cross-section shapes.

Hence, it is possible to focus on the most important contribution of this work, which is closely related to the determination of the optimized geometrical project for surrounding-gate devices, taking into consideration the different cross-section shape alternatives. Bearing in mind this objective, it is extremely important to notice that the circular-shaped ones presented the lowest subthreshold slope values while the square-shaped showed the highest ones.

Remembering that a lower S value represents a better performance in terms of channel control by the gate and short channel effects, the curves in figure 2 show a very interesting influence of the cross-section shape. As it is clear from the graph, MuGFET devices tend to present a better behavior (less short channel effects) as the number of sides of the cross-section shape increases. The same tendency was observed for threshold voltage.

Figure 3 shows the potential distribution in the middle of the channel for surrounding gate MuGFETs of $L=20\text{nm}$ with square section (3.A), octagonal section (3.B) and circular section (3.C). It is possible to see that the best potential uniformity near the gate is obtained by the circular gate.

Figure 4 shows the potential comparison among these three different structures in the middle of Y position for $V_{GS} = 0.4\text{V}$ (a little bit lower than V_{th}), and it is possible to see that when the number of the gates increases the potential at the center of the channel is lower, i.e., more controlled by the gate and present less influence of the drain voltage through the channel (better short channel effects).



(A)

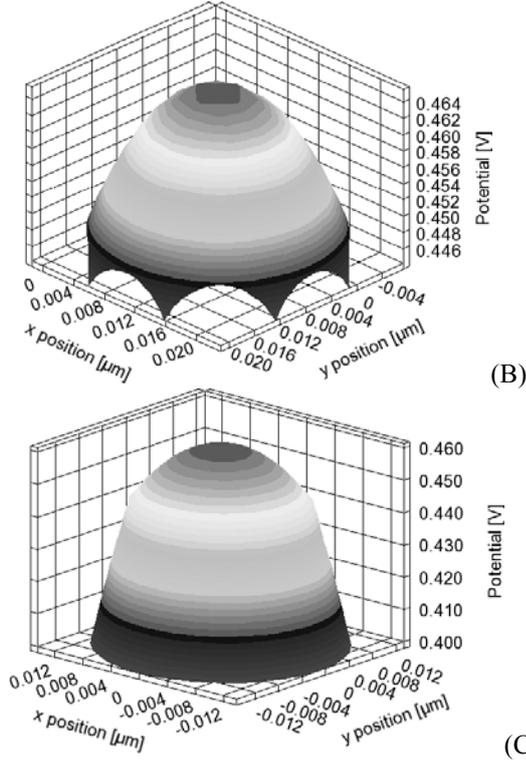


Figure 3: Potential distribution in the middle of the channel ($Z=L/2$, where $L=20\text{nm}$) for square section (A), octagonal section (B) and circular section (C).

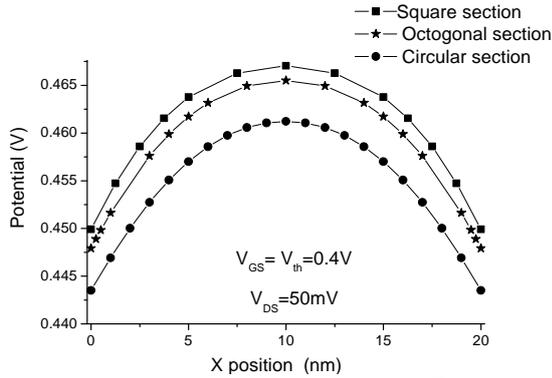


Fig. 4: The potential comparison among these three different structures in the middle of Y position is presented in (D) for $V_{GS} = 0.4\text{V}$.

4.2. Comparison between surrounding-gate devices with different vertical physical features

In order to investigate how the vertical physical dimensions influence the impact of the cross-section shape on the devices performance, two extreme cases of surrounding-gate transistors, namely with circular and square channel sections, were selected in the next step of this work.

To begin with the theoretical approach, it is worth remembering that this work makes use of the natural length concept, which is closely related to the maximum accepted channel length reduction that avoids the short channel effect [6]. According to literature, the natural length parameter for square and circular section devices is given by λ_{square} and $\lambda_{\text{circular}}$, as it is shown in equations 1 and 2, respectively.

$$\lambda_{\text{square}} = \sqrt{\frac{\epsilon_{\text{Si}} \cdot t_{\text{Si}} \cdot t_{\text{ox}}}{4\epsilon_{\text{ox}}}} \quad (\text{eq. 1})$$

$$\lambda_{\text{circular}} = \sqrt{\frac{2 \cdot \epsilon_{\text{Si}} \cdot t_{\text{Si}}^2 \cdot \ln\left(1 + \frac{2 \cdot t_{\text{ox}}}{t_{\text{Si}}}\right) + \epsilon_{\text{ox}} \cdot t_{\text{Si}}^2}{16 \cdot \epsilon_{\text{ox}}}} \quad (\text{eq. 2})$$

where t_{Si} is the silicon thickness, ϵ_{Si} is the silicon permittivity, ϵ_{ox} is the oxide permittivity and t_{ox} is the gate oxide thickness.

In order to express these parameters as a function of the gate oxide thickness (t_{ox}) and silicon film thickness (t_{Si}) ratio, the ‘‘K factor’’ was defined as it is shown in equation 3.

$$K = \frac{t_{\text{ox}}}{t_{\text{Si}}} \quad (\text{eq. 3})$$

Therefore, considering the numerical values as it is mentioned in equations 4 and 5, it was possible to write expressions for λ_{square} and $\lambda_{\text{circular}}$ for a particular t_{Si} as a function of the ‘‘K factor’’ (equations 6 and 7 respectively).

$$\epsilon_{\text{ox}} = 3.9\epsilon_0 \quad (\text{eq. 4})$$

$$\epsilon_{\text{Si}} = 11.7\epsilon_0 \quad (\text{eq. 5})$$

$$\frac{\lambda_{\text{square}}}{t_{\text{Si}}} = \sqrt{0.75K} \quad (\text{eq. 6})$$

$$\frac{\lambda_{\text{circular}}}{t_{\text{Si}}} = \sqrt{0.375 \ln(1 + 2 \cdot K) + 0.0625} \quad (\text{eq. 7})$$

Based on this mathematical approach, the same procedure of extracting the subthreshold slope and the threshold voltage was performed for other values of K, obtained by varying the gate oxide thickness (t_{ox}) from 2 to 12 nm and keeping the silicon film thickness (t_{Si}) constant as 20 nm. Consequently, ‘‘K factor’’ ranged from 0.1 to 0.6, a wide variety considering the t_{ox} and t_{Si} usual fabrication rate.

The curves of subthreshold slope as a function of the channel length ($S \times L$) for three different K values are displayed in Figure 5.

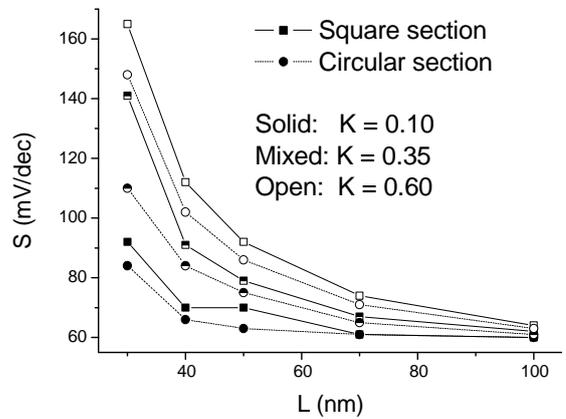


Fig. 5: Subthreshold slope of square and circular cross-section transistors for three different values of $K = t_{\text{ox}}/t_{\text{Si}}$ parameter.

The first relevant conclusion is that, for the whole analyzed K range, circular section devices presented always better behavior than square section ones. Therefore, comparing transistors with the same silicon and oxide film thickness but with different cross-section shapes, the circular structure tends to present the best control of the channel region by the gate for all range of L studied.

It is also possible to extract from the graph that the devices with higher K values (and consequently higher t_{ox} values) offered a worse channel current control as a result of the higher average distance between the gate and the channel center.

Following the same procedure than in the first part of the current work, it is possible to focus on the threshold voltage dependence on the channel length, as it is shown in figure 6 for the case of $K = 0.6$.

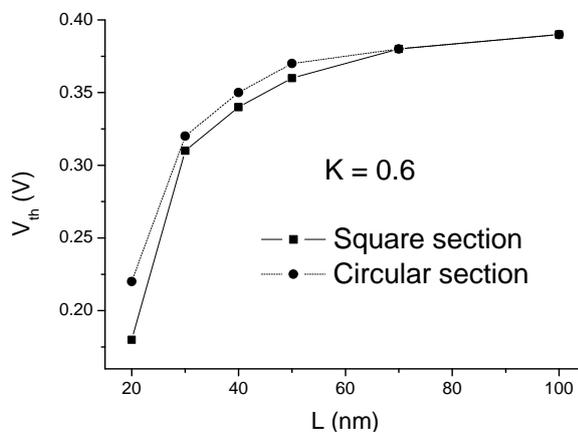


Figure 6: Threshold voltage for square and circular cross-sections transistors for different gate lengths

Analyzing the plotted curves, it is possible to extract the same performance tendencies that had already been observed in the subthreshold slope analysis, which was based on Figure 5.

Once more, circular section devices presented a better behavior, expressed by the less susceptibility to short channel effects. Square section transistors presented a more relevant threshold voltage variation as the channel length became very short.

5. CONCLUSIONS

In this work, the cross-section shape influence on surrounding MuGFETs was highlighted. By analyzing curves of subthreshold slope and threshold voltage as a function of the channel length, it was possible to evaluate and compare the applicability of the multiple-gate structures with different cross-section shapes.

In the first part, surrounding gate devices with square, octagonal and circular channel sections were selected and compared to each other and to the already specified double-gate structure. First of all, the reliability of the simulation data was checked by verifying the performance enhance obtained with surrounding-gate devices in comparison to double-gate ones.

Besides that, it is quite important to lay stress on the main contribution of this work, namely the comparison of the different cross-section shapes and, eventually, the definition of the most suitable geometrical feature. According to the obtained results, it was possible to notice that MuGFET devices tend to present a better performance as the number of sides of the cross-section shape increases. In other words, the circular shape, which presents a lower average distance between the channel center and the gate for a specific t_{Si} , may be considered the most suitable geometric shape in terms of channel current control.

The second part of the work focused exactly on widening the horizons of this analysis by evaluating the cross-section shape influence dependence on the physical features. This analysis was performed by varying the oxide film thickness in a way of changing the “ K factor” value, which was previously defined during the mathematical approach of the “natural length” concept.

The obtained results showed the same tendencies that were verified in the first step of the work, even for a K value 6 times higher. The circular shape device presented a better behavior in terms of subthreshold slope and threshold voltage, meanwhile for both cross-section shapes, the increase in the K value deteriorated the devices performance.

Taking all the mentioned points into consideration, it is possible to conclude that the study of the cross-section shape influence on MuGFETs may be interpreted as a natural sequence to the previous development from single-gate to multiple-gate devices. By analyzing the obtained results from a global point of view, the devices tend to present a better performance as the number of sides of the cross-section shape increases, an important conclusion as a first approach on such a promising technological issue.

6. ACKNOWLEDGEMENTS

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7. REFERENCES

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