2-INPUT NEUROMORPHIC AND LOGIC GATE BASED ON INTEGRATE-AND-FIRE NEURON USING CMOS TECHNOLOGY

Leonardo Enzo Brito da Silva, Fernando Rangel de Sousa

μEEs/DEE/CT – Federal University of Rio Grande do Norte,
Campus Universitário, Lagoa Nova, 59072970, Natal – RN, Brazil
Phone:+558432153910, e-mail: leonardoenzob@gmail.com , rangel@ieee.org

ABSTRACT

This paper presents a report of a simple neural network implementation that performs a 2-input AND bolean operation. The corresponding neuromorphic circuit is based on the integrate-and-fire neuron and was realized in CMOS 0,5μm technology.

1. INTRODUCTION

The downscaling of semiconductor device dimensions, which results in the degradation of their reliability, has lead to the need of new approaches for fault-tolerant design methods [1]. Therefore, in order to increase the performance and the robustness of electronic circuits, as well as to reduce power consumption, biologically inspired circuit topologies (also known as neuromorphic circuits) are being considered. Hence, artificial neural networks along with transistor operation in the weak inversion region have found application in fault-tolerant systems and low-power consumption systems[2,3].

In this context, this paper presents an implementation of a 2-input CMOS neuromorphic AND logic gate based on a classical spiking neuron: the integrate-and-fire neuron [4]. The circuit implemented was taken from [5, 6], but it can also be found in an alternative design in [7]. The advantage of the architecture chosen is its very compact design.

The work presented here has been carried out by an undergraduate student in a scientific initiation program.

2. 2-INPUT NEUROMORPHIC AND LOGIC GATE

The neuromorphic logic gate is based on the neural network shown in Figure 1.

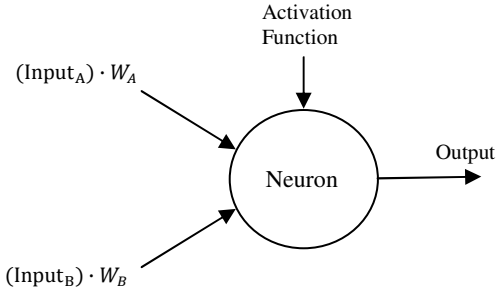

Figure 1: Simple neural network formed by a single neuron.

The function performed by the neuron depends on the values chosen for the weights W_A and W_B as well as on the kind of activation function. In order to implement an AND logic, the weights W_A and W_B that multiplies each input are unity, and a threshold activation function was chosen.

Thus, the neuromorphic AND is divided into two major blocks: the conversion block, that modifies the binary input accordingly to the nature expected in the neuron, and the neuron block, which decides on the most suitable output. These blocks are depicted in detail in the subsequent topics.

2.1. Integrate-and-Fire neuron overview

The integrate-and-fire neuron model is depicted in Figure 2. A sum of current inputs is integrated through the charging path and then compared to the value of a threshold function. If the output of the integrator exceeds the threshold value, the comparator output is at maximum; otherwise, it remains at a minimum. The switch block toggles between the charging and discharging paths depending on the value of the integrate-and-fire output that is fed back: the reset block will be enabled right after a maximum output from the comparator, otherwise will be disabled.

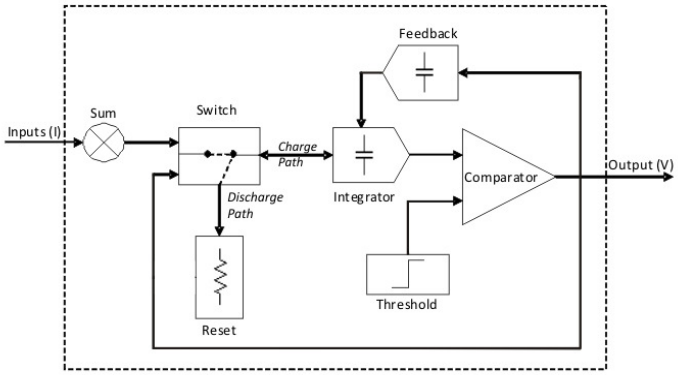

Figure 2: Integrate-and-fire neuron model. The integrator block is formed by a capacitor as well as the feedback block. The switch and reset blocks are implemented with transistors.

Figure 3 depicts the integrate-and-fire neuron electronic circuit. The input current I_{in} is integrated on the capacitor C_1, what leads to an increase of the voltage in its terminals. When the voltage across the capacitor reaches the switching point of the inverter, V_{out} = VDD. The capacitor C_2 ensures the secure switching of the

circuit. During a pulse, C_1 discharge path (through the transistors $M_{n\_disch\_1}$ and $M_{n\_disch\_2}$) is enabled and the charging path (through the transistor M_{p_in}) is disabled.

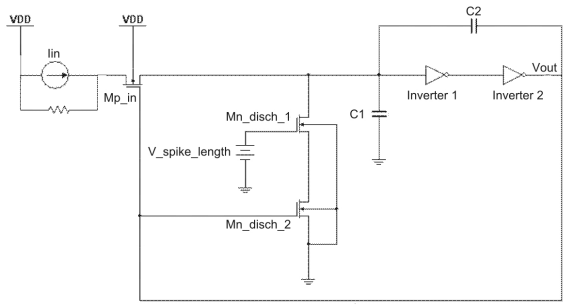

Figure 3: Schematic of the integrate-and-fire neuron electronic circuit. The value of $V_{\_spike\_length}$ is equal to VDD.

Then, the voltage across C_1 decreases and V_{out} switches back to ground potential. At this point the charging and discharge paths of the capacitor C_1 are opposite of those previously mentioned, and the cycle starts again. The width of the pulse is controlled by the voltage $V_{\_spike\_length}$ (one is inversely proportional to the other), and the spike firing rate is proportional to I_{in} intensity.

Table 1 shows the lengths and width of the integrate-and-fire neuron transistors, used in the 2-input neuromorphic AND logic gate.

Transistor	W(μm)	L(μm)
M_{p_in}	1	1
$M_{n\_disch\_1}$	1	25
$M_{n\_disch\_2}$	1	25
NMOS (Inverter 1)	40	25
PMOS (Inverter 1)	1	25
NMOS (Inverter 2)	5	2
PMOS (Inverter 2)	15	2

Table 1: lengths and widths of the transistors used in the integrate-and-fire circuit. The dimensions of the inverters 1 and 2 were chosen in order to make their switching threshold voltage 1V and 2.5V, respectively.

The capacitance of C_1 and C_2 are 5pF and 1pF respectively.

From now on, the integrate-and-fire neuron building block will be designated as in Figure 4. The I&F block is not the neuron represented in Figure 1: it is enclosed in the latter.

Figure 4: Integrate-and-fire block.

2.2. Conversion Block

The conversion block is responsible for transforming the voltage level from the binary inputs into voltage spikes, and then source it to the neuron block. Figure 5 shows the conversion diagram.

As depicted in Figure 6, this block is implemented using a current mirror that sources two constant currents at the transistors M2 and M3, and transistors that function as switches (M4 and M5), which are open when the logic level from the binary input (INPUT_A, INPUT_B) is 1 and closed when it is 0.

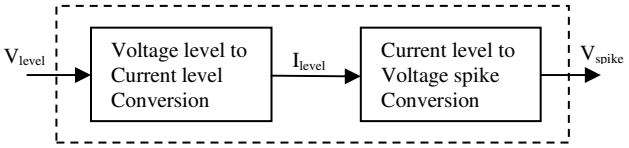

Figure 5: Conversion Block.

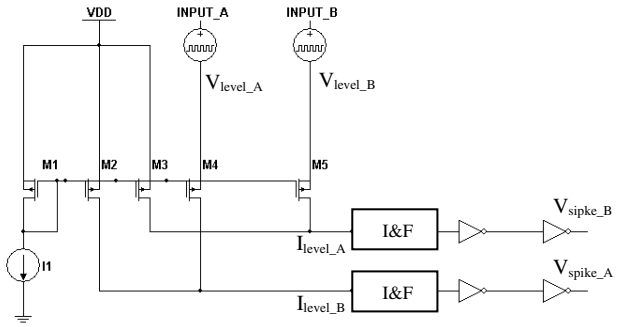

Figure 6: Schematic of the input conversion block circuit.

When conducting, these transistors source a current based on Equation 1:

$$I_i = I_1 \cdot \frac{W_i}{W_1} \quad ; \quad i=\{2,3,4,5\} \quad (1)$$

Where the subscript 1 refers to the transistor M1, and the subscript i refers to the all the other transistors, viz. M1, M2, M3, M4 and M5. The W stands for the width of the depletion channel. The lengths of all the above transistors are equal. I_1 is the current source that supplies the reference current to the current mirror.

The total current of each integrate-and-fire minor block will have two components, although it leads to more power consumption: this way, even if the logic level of the binary input is low, the total current will not be zero.

The transistors' lengths and widths are listed in the Table 2.

Transistor	W(μm)	L(μm)
M1	10	10
M2	3	10
M3	3	10
M4	10	10
M5	10	10
NMOS (inverters)	5	10
PMOS (inverters)	15	10

Table 2: lengths and widths of the transistors from the input conversion block.

The two inverters used after the integrate-and-fire minor blocks aim to restore the maximum and minimum voltage values from which the spikes occur. It is desirable to assure that when spikes are not fired, the voltage should be zero, otherwise it should be VDD - for some values of the input current, until the spikes begin to be

released, a DC value is generated in the minor integrate-and-fire block output.

For a voltage supply VDD of 5V and a current source I_1 of 1nA, the results of the 1s transient simulation of this block is shown in Figure 7.

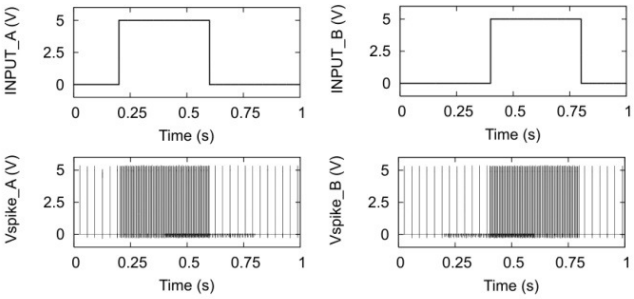

Figure 7: Voltage signals representing the binary inputs A and B as well as the voltage spikes representing the outputs V_{spike_A} and V_{spike_B}.

2.3. Neuron Block

Although the neuron block conventionally starts at a sum block, the transformation of the voltage spikes from the conversion block output into current spikes will be included - for comprehension purposes it will not be separated from the sum block. The Neuron Block is then, represented in the Figure 8, by two major blocks.

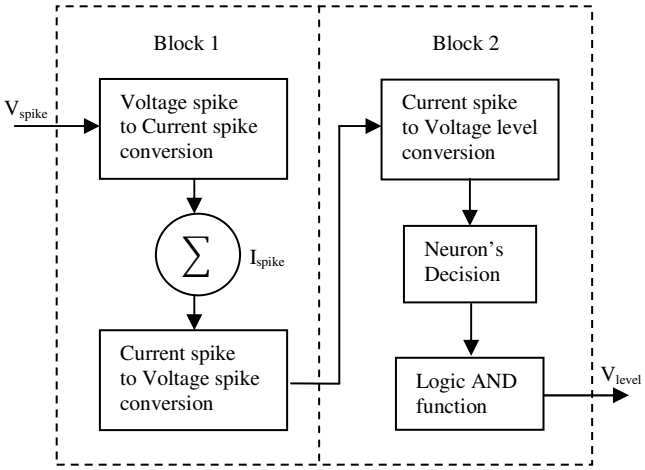

Figure 8: Neuron Block and its minor blocks 1 and 2.

Block 1 is responsible for the conversion between voltage spikes (V_{spike_A} and V_{spike_B} – see Figure 6) and current spikes (which flows through the transistors M9 and M10 sources – see Figure 9). The analysis is similar to that made for the circuit in Figure 6. It also has the function of summing the currents, represented by the common source node of the transistors M9 and M10. The current spikes are then fed into the input of the third integrate and fire minor block, which releases voltage spikes.

The two inverters used in the output of the circuit have the same purpose as those found at the conversion block.

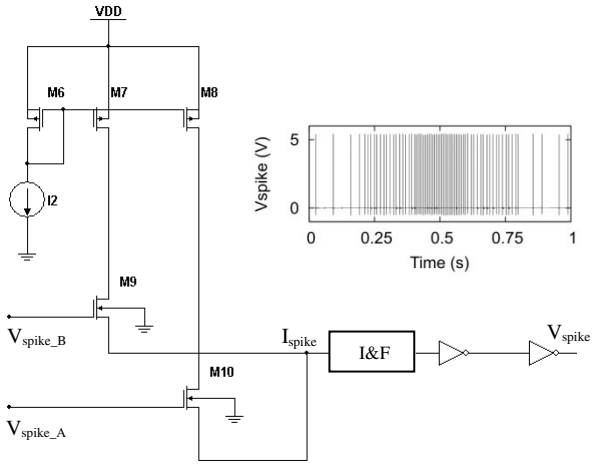

Figure 9: Block 1 circuit schematic and its output during a transient simulation with the same stimuli used in Figure 7: the signal V_{spike}.

Due to the fact that I_{spike} has a smaller rms value than I_{level_A} and I_{level_B}, the current source I_2 must than supply a higher current than I_1. Two current sources and current mirrors were chosen, instead of one each so as to allow the sweeping of a wider range of current combinations within feasible transistor widths (according to Equation 1). For I_1 and I_2 equal to 0.5µA and 1nA, respectively, the result of the 1s transient simulation can be evaluated from the graphic in Figure 9.

Block 2 is responsible for converting the voltage spike output from Block 1 into voltage level. Furthermore, it also contains the neuron's decision function. Figure 10 shows the schematic of the electronic circuit.

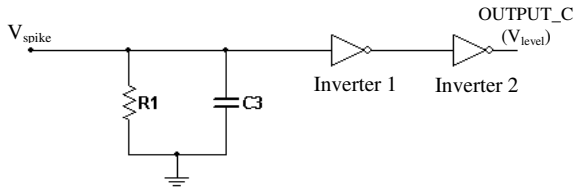

Figure 10: Block 2 circuit schematic, where R1=100kΩ and C3=0.1µF.

The neuron decision system is based on the switching point of the first inverter. It is implemented in order to generate an AND logic by obeying a threshold function whose value is compared to the input of this inverter, which depends on the spike density of the voltage V_{spike}, that is similar to the spike density of the current I_{spike}.

The second inverter is responsible for restoring the logic levels, thus matching the voltage level of OUTPUT_C to those of INPUT_A and INPUT_B.

Figure 11 depicts in the first graphic the voltage across the capacitor C_3 terminals and the value of the neuron activation function. The second graphic shows the system output, for the same inputs of Figure 6, and with currents I_1 and I_2 equal to 2µA and 5µA respectively.

Figure 12 reveals the transfer characteristic V_{out} versus V_{in} of the inverter 1.

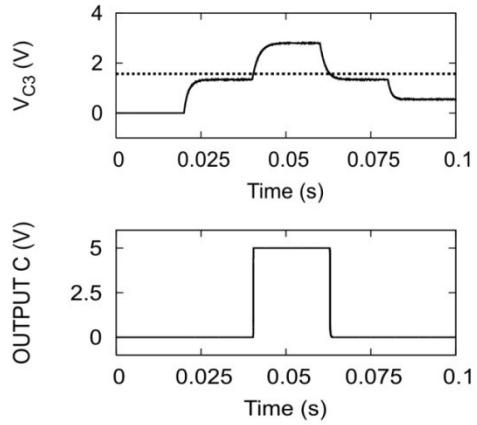

Figure 11: For a transient simulation of 0.1s, the voltage across the capacitor C_3 and the threshold value of approximately 1.6V is shown in the upper graphic. The lower graphic is the AND logic result of this implementation.

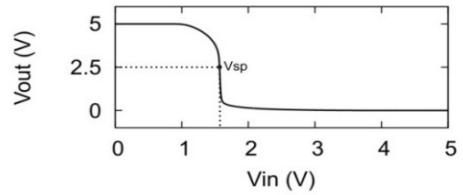

Figure 12: Inverter 1 transfer characteristic. The voltage switching point is 1.5686V.

The transistors' lengths and widths of the neuron block are listed in Table 3.

Transistor	W (μm)	L (μm)
M6	30	10
M7	30	10
M8	30	10
M9	30	10
M10	30	10
NMOS (Inverters from Block 1)	5	10
PMOS (Inverters from Block 1)	15	10
NMOS (Inverter 1 from Block 2)	2	2
PMOS (Inverter 1 from Block 2)	1	2
NMOS (Inverter 2 from Block 2)	1	2
PMOS (Inverter 2 from Block 2)	3	2

Table 3: lengths and widths of the transistors from the neuron block.

As can be seen from Figure 11, the voltage across the capacitor C3 only reaches a considerable value when currents significantly higher than those from Figure 6 are supplied by I_1 and I_2. Another concern is the capacitance of C3, which is considerably high. Options to implement it involve active circuits such as transconductance amplifiers.

3. CONCLUSIONS

This paper demonstrated the implementation of a 2-input neuromorphic AND logic gate, as well as simulations' results. In order to facilitate the circuit's overall comprehension, the voltage signals were tracked through the circuit at different nodes, thus showing the level versus spike conversions.

The chosen circuit topology does not include the fault-tolerance property, as it would be necessary a more complex multi-layer neural network. It has also proven itself power consuming and with a high prospective layout area, due to the number of elements and to the capacitance values, particularly that from C3.

Since the research is in process of development, other topologies will be considered so as to reduce power consumption (transistor operation in subthreshold), size and number of transistors, as well as resistance and capacitance values.

Therefore, the optimization of the presented electronic circuit, along with the layout development is subject of ongoing research at the Federal University of Rio Grande do Norte.

4. ACKNOWLEDGEMENT

The authors are grateful to PROPESQ and to CNPq for supporting this research, as well as the μEEs, for providing the environment and making this work possible.

5. REFERENCES

[1] N. Joye, A. Schmid, Y. Leblebici, T. Asai, and Y. Amemiya, "Fault-Tolerant Logic Gates Using Neuromorphic CMOS Circuits", IEEE, *IEEE 3rd Conference on Ph.D. Research in Microeletronics and Eletronics*, pp. 249-252, 2007.

[2] S. Aunet, and V. Beiu, "Ultra Low Power Fault-Tolerant Neural Inspired CMOS Logic", *2005 IEEE International Joint Conference on Neural Networks*, Vol. 5, pp. 2843-2848, 2005.

[3] A. Schmid, Y. Leblebici, "Robust and fault-tolerant circuit design for nanometer-scale devices and single-electron transistors", IEEE, *2004 IEEE International Symposium on Circuits and Systems*, pp. 685-688, Vol. 3, 2004.

[4] R. Wells, "The integrate-and-fire neuron model as a sensory neuron model", *Technical report*, University of Idaho, pp. 1-13, 2003.

[5] J. Lazarro, "Low-power silicon spiking neurons and axons", IEEE, *1992 IEEE International Symposium on Circuits and Systems*, pp. 2220-2223, Vol. 5,1992.

[6] J. P. Abrahamsen, P. Häfliger, T. S. Lande, "A time domain winner-take-it-all network of integrate-and-fire neurons", IEEE, *2004 IEEE International Symposium on Circuits and Systems*, pp. 361-364, 2004.

[7] G. Indiveri, "A low-power adaptative integrate-and-fire neuron circuit", IEEE, *2003 IEEE International Symposium on Circuits and Systems*, pp. 820-823, Vol. 4, 2003.

[8] R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, Wiley-IEEE Press, 2nd Edition, 2008.

[9] S. Haykin, *Neural Networks: A Comprehensive Foundation*, Prentice Hall, 2nd Edition, 1998.

[10] G. W. Roberts, A. S. Sedra, *Spice*, Oxford University Press, 2nd Edition, 1996.

[11] S. Liu, J. Kramer, G. Indiveri, T. Delbück, R. Douglas, *Analog VLSI: Circuits and Principles,* MIT Press, 2002.