LAYOUT, MANUFACTURE AND EXPERIMENTAL CHARACTERIZATION OF THE OCTO MOSFET

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ABSTRACT

Thinking in scalability (die area reduction) of the Diamond SOI MOSFET, a new layout style is proposed, entitled as OCTO MOSFET (OM). The OCTO geometric shape of the gate is octagonal in contrast to the Diamond transistor that is hexagonal. This new proposal allows improvements in terms of die area, drain current and transconductance. IC Station (Mentor Graphics) is used to implement the OCTO layout and an inverter circuit following the design rules of the 0,35 µm AMI (On-Semiconductor). These devices were manufactured via MOSIS Educational Program (MEP) and experimental characterization was performed showing the feasibility of the proposed idea and reached a better performance than the pre-existent conventional ones.

1. INTRODUCTION

Nowadays, several works have been shown us that there are still many improvement opportunities considering the planar MOSFET technology, while new technologies of the non-planar transistors has been heavily investigated by using Silicon-on-Insulator (SOI) wafers, such as FinFETs, Multi-gates, Pillar Surround Gate and Cynthia in order to enhance the transistor electrical performance [1]. Some examples of that are circular gate MOSFETs (CGT) operating in the external drain bias configuration [2], overlapping-circular gate transistor (O-CGT) [3], Wave [4] and Diamond [5] transistors.

Particularly, the Diamond transistor was designed in order to use the corner effect [1] in the longitudinal (parallel) direction of the channel ("drain/channel/source engineering") to improve the longitudinal electric field (ε_x), consequently the channel mobile carriers velocity (v_x), the drain current (I_{DS}) and the transconductance (g_m) and to reduce the on-state series resistance (R_{DSon}), due to the drain voltage (V_{DS}) applied to the hexagonal gate geometric shape [5]. As Diamond structure presents a channel length (L) larger than that found in the equivalent conventional one, their use is limited for the digital integrated circuits applications [5]. In order to overcome the scalability issue (die area reduction), OCTO layout style was created by cutting the beaks of the hexagonal geometry of Diamond, as indicated in Figure 1, generating an octagonal geometric shape of the gate. This new structure is also able to enhance the resultant longitudinal (parallel) electric field ($\vec{\varepsilon}$) over the channel.

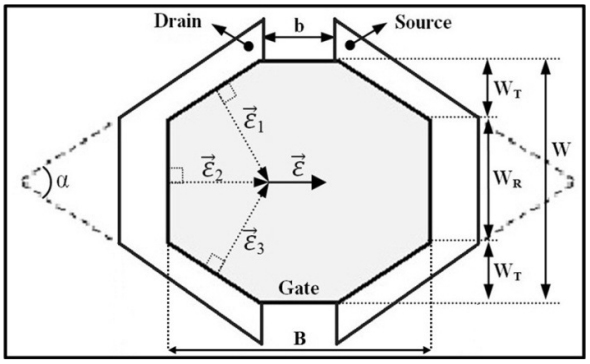

Figure 1 – Superior view of OM.

In Figure 1, the parameters W, W_T and W_R are the channel widths of the OCTO MOSFET (OM) of the trapezoidal and rectangular parts that compose the octagonal geometric shape, respectively, B and b are the largest and smallest distance between the drain and the source regions, respectively, α is the angle between the sides of the hexagonal geometric shape that belongs to the junctions of the drain/silicon film and silicon film/source regions; $\vec{\varepsilon}_1$, $\vec{\varepsilon}_2$ and $\vec{\varepsilon}_3$ are the longitudinal (parallel) electric field components due to the drain voltage (V_{DS}) that is applied on each side of the drain/silicon film regions, and $\vec{\varepsilon}$ is the resultant longitudinal electric field given by the vector sum of these three electric field components ($= \vec{\varepsilon}_1 + \vec{\varepsilon}_2 + \vec{\varepsilon}_3$), that is larger than that one found in the conventional counterpart, considering the same W/L and bias conditions.

2. LAYOUT IMPLEMENTATION

To implement the layout of the OM, it was used the software IC Station (Mentor Graphics) [6], by using the design rules of the 0.35 µm AMI (On-Semiconductor) manufacturing process, available in the MOSIS Educational Program (MEP).

For this project, twelve masks were used: active region, polysilicon, active contact, polysilicon contact, via1, via2, metal1, metal2, metal3, nwell, pselect and nselect.

In Figure 2, is shown a comparison between the layout of a p-channel conventional MOSFET (CM) (Figure 2.a) and an n-channel OM (Figure 2.b). The dimensions for both devices are depicted in Table 1.

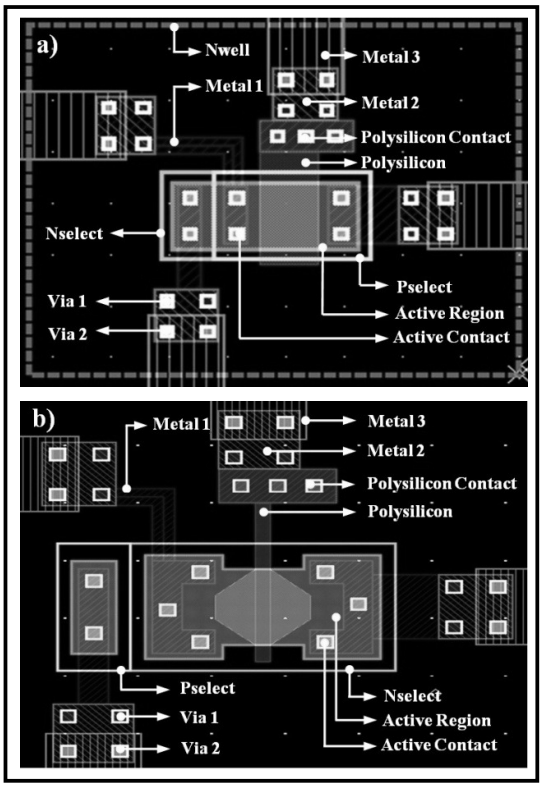

Figure 2 – p-channel CM (a) and n-channel OM (b) Layouts.

Table 1 – p-channel CM (a) and n-channel OM dimensions.

	W (µm)	L (µm)	B (µm)	b (µm)	α (º)	W_R (µm)
CM	6.0	7.0	-	-	-	-
OM	6.0	3.5	4.0	1.0	53.1	4.5

In Figure 3 presents two layout examples of the inverters (NOT) logic circuit implemented with CM (Figure 3.a) and OM (Figure 3.b).

3. OCTO MOSFET CHARACTERISTICS

Analyzing the equivalent circuit of OM is possible to understand that this device is given by three transistors connected in parallel: two with trapezoidal geometric shape and one with rectangular geometric shape. Each transistor presents a channel length (L_{eff_T} and L_{eff_R}) and a width (W_T and W_R). The OM geometric factor $[(W/L)_{OCTO}]$ is given by the equation (1), where L_{eff_T} is considered, in first approximation, equal to (B+b)/2.

$$\left(\frac{W}{L}\right)_{OCTO} = \frac{4W_T B + W_R(B+b)}{B(B+b)} \qquad (1)$$

The channel widths of the rectangular (W_R) and two trapezoidal (W_T) transistors that compose the octagonal geometric shape are given by W-2W_T and [(B-b)/2]tan(α/2), respectively. The effective channel length (L_{eff}) of the OM device can be obtained by $W/(W/L)_{OCTO}$.

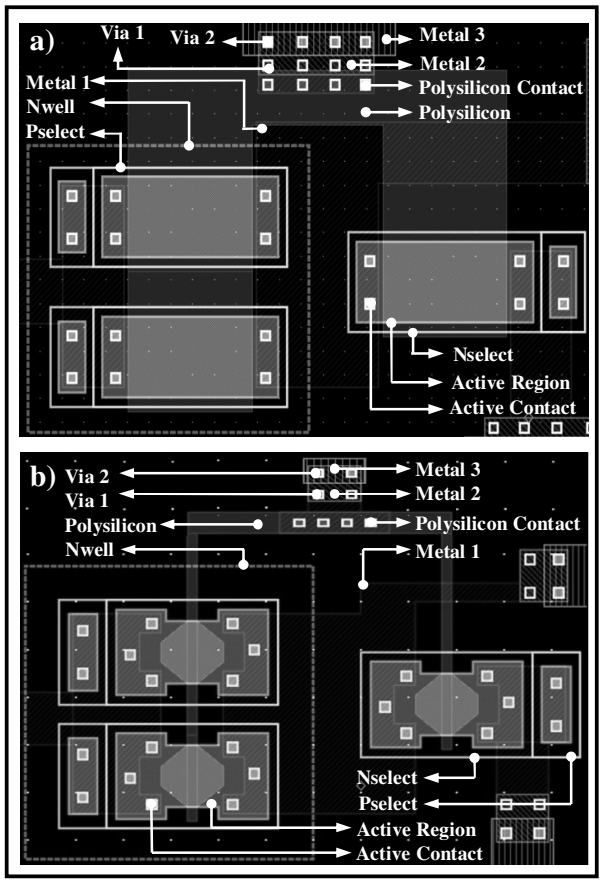

Figure 3 – Two layouts of the inverters (NOT) logic circuits by using CM (a) and OM (b), respectively.

4. EXPERIMENTAL RESULTS

Several conventional and OCTO MOSFETs were manufactured with 0.35 µm AMI (On-Semiconductor) manufacturing process, available in the MOSIS Educational Program (MEP).

In Table 2 are indicated the CM and OM manufactured transistors dimensions.

Table 2 – Transistors dimensions for α = 36.9º.

Shape	W	L_{eff}	W/L	B	b	Gate Area	Area Gain
OM1	17.0	25.0	0.681	41.0	3.0	$456\lambda^2$	5.79%
OM2	17.0	20.3	0.838	28.5	3.0	$376\lambda^2$	22.3%
OM3	17.0	13.6	1.250	16.0	3.0	$244\lambda^2$	49.6%
CM	17.0	28.5	0.596	-	-	$484\lambda^2$	-

* W, L_{eff}, B and b are given in λ=0.35 µm.

Figure 4 presents the experimental results of $I_{DS}/(W/L)$ versus V_{GT} for V_{DS}=0.2V. I_{DS} was normalized in relation of W/L in order to remove the influence of the devices dimensions. They were put as a function of V_{GT}

in order to remove the influence of different V_{TH} between these devices.

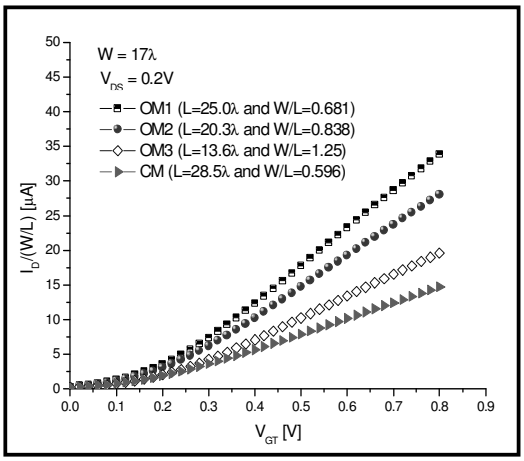

Figure 4 – $I_{DS}/(W/L)$ x V_{GT} for V_{DS}=0.2V.

Analyzing Figure 4, we can observe that all OM are able to produce larger $I_{DS}/(W/L)$ values than that found in the conventional for a specific V_{GT} and for each operation regions (subthreshold, saturation and triode), even that OCTO MOSFETs present higher geometric factors. These OM $I_{DS}/(W/L)$ behaviors are justified due to the higher longitudinal electric fields in these devices than those found in the CMs. Note that OM3 can produce larger $I_{DS}/(W/L)$ than CM, indicated in Table 2, with approximately half of the CM die area.

Figure 5 presents the g_m versus V_{GT} curves for V_{DS} equal to 0.2V of the CM and OM.

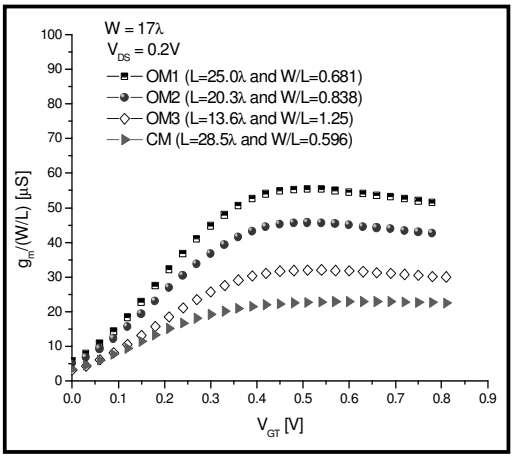

Figure 5 – $g_m/(W/L)$ versus V_{GT} for V_{DS}=0.2V.

Table 3 presents the maximum transconductances of the CM and OM that were extracted of the curves presented in Figure 5.

Table 3 – Octagonal and Conventional MOSFETs maximum transconductances for V_{DS}= 0.2V.

Shape	g_m [µS]	Comparisons with CM (+ improvement, - worsening)
OM1	55.4	+142%
OM2	45.7	+99.6%
OM3	32.1	+40.2%
CM	22.9	0.00%

Note that OM maximum transconductance is always higher than that presented in CM, due to the higher longitudinal electric field. Additionally, by using OM3 instead CM counterpart, we can obtain a maximum transconductance 40.2% higher than that found in CM counterpart and therefore OCTO layout style becomes another alternative to be used in analog integrated circuits applications, allowing a significant die area reduction.

5. CONCLUSIONS

This paper presented a new structure named OCTO MOSFET that also explore the corner effect in the longitudinal direction of the channel to improve the parallel electric field along of the channel and consequently improve the drain current and transconductance. Experimental results prove that OCTO layout style can be used in order to improve the performance (drain current and transconductance) of analog integrated circuits application (drivers and amplifiers) with a important die area reduction.

6. REFERENCES

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