TEST STRUCTURES FOR CHARACTERIZATION OF LOCAL RANDOM VARIABILITY IN 65NM CMOS BULK TECHNOLOGY

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ABSTRACT

Process variations impose an important challenge to future nano-scaling of VLSI technology. In this work, we describe test structures at 65nm feature size aimed to investigate and characterize truly local random variations. The first test structure is a MOSFET matrix-style like with closely identical designed transistors. The second and third structures are based on a procedure to measure an array of stacked-pairs of MOS transistors. A test chip design was completed in IBM 65nm CMOS bulk technology and the final chip area is about 1580 x 1580µm.

1. INTRODUCTION

For the past several years, variation in CMOS process has been a concern in the design, manufacture and accurate operation of integrated circuits. Nowadays, intradie variations (for further discussion on the difference between interdie and intradie variation see ref. [1]), are considered as one of the limiting factors for further CMOS scaling [2] and certainly a drawback to the continuance of Moore's law [3]. Intradie fluctuations originate mainly from the spatial distribution of fewer impurity atoms in the gate depletion layer, which is determined by a stochastic process [4, 5]. That is, this type of characteristics fluctuation cannot be controlled in principle. Mismatch differences among MOSFETs are of utmost concern, since the fluctuation of their characteristics becomes significant as their physical sizes decrease. In figure 1, is presented an example of this variation, showing the I_{DS}-V_{GS} curve for linear region MOS transistor regime. For that case, in figure 2 it is shown the histogram of 1000 samples of the threshold voltage of the above characteristic.

Therefore, to model and to characterize these variations, high accuracy measurement data on local variability are needed to provide mismatch transistor models [6, 7] with realistic statistical data. Thus, one of the most serious challenges in process variations for sub-100-nm technologies is the effective and reliable way to obtain statistical data from FETs within reasonable time. Due to their statistical random nature, local random variation effect must be characterized by measuring a large number of individual devices and special care must be taken concerning the test structure and the measurement setup. A basic approach to obtain statistical data from a given process is to use arrays of identical transistors [8, 9]. Transistor arrays unavoidably occupy a large area and require sequentially long measurements, reducing the measurement throughput. Nevertheless, the attractiveness of transistor arrays as test structures has led to recent efforts [10] that aim at creating optimized structures for fast and semi-automatic measurement procedures. Our structures rely on a multiplexed transistor array with high-density access to multiple devices by means of address decoding and access circuits. Another alternative for variability measurement is to use a common gate series-connected MOSFET structure [11-

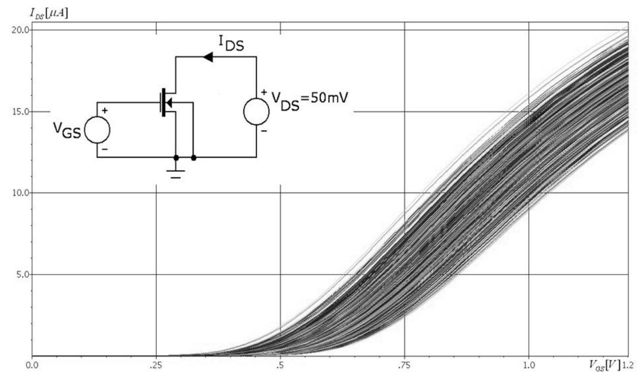

Figure 1 – I_{DS}-V_{GS} variation due to local random variability.

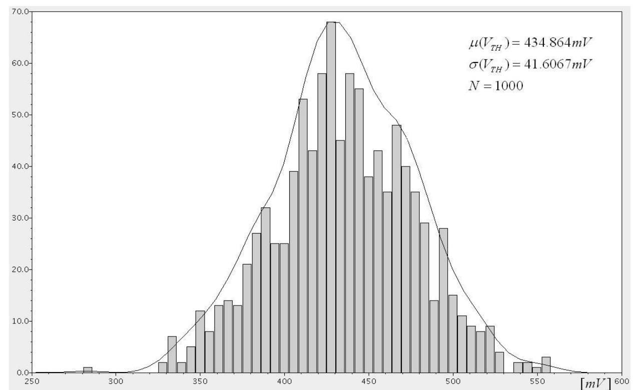

Figure 2 – Threshold voltage variation histogram.

13] suitable for process monitoring purposes. In this structure the mismatch behavior of a large number of MOSFETs pairs is promptly evaluated in as small area as possible. In this paper we propose a test chip designed with new structures for local random variability measurements. Design, simulation and variance simulations by Monte-Carlo, were done for a state of the art 65 nm CMOS bulk process. The designed test chip has the following test structures:

- A MOSFET matrix-style array composed of multiplexed/biased closely spaced identical MOS transistors.
- An array of MOSFET stacked-pairs on which their gates are internally connected.
- An array of MOSFET stacked-pairs in which their gate are externally connected, providing the possibility to evaluate layout/distance mismatch.

In session 2 we present the MOSFET Matrix. In section 3 the two versions of the MOSFET stacked-pair matrix are shown. Section 4 presents an overview of the test-chip under fabrication. Finally, section 5 presents the conclusions from this work.

2. A MOSFET MATRIX

The purpose of this structure is to evaluate the mismatch between transistors in the traditional way (data analysis of current-voltage curves). Based on [9], the MOSFET Matrix includes bias circuitry, level shifters and address decoding. The transistors are arranged in an individually addressable fashion. The structure contains a total of 2048 devices (1024 NMOS and 1024 PMOS) placed in 64 columns with 32 rows. Eight groups of eight different size transistors compose the MOSFET Matrix. *Kelvin* measurement technique is used to minimize the effects of these IR drops. The manner as each transistor is connected and how our Kelvin technique (force and sense lines) selects a device is shown in the following figure 3(a) and 3(b).

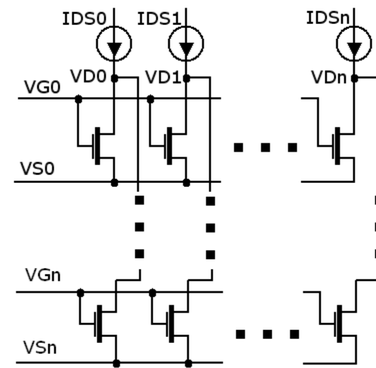

Figure 3(a) – Transistor connection.

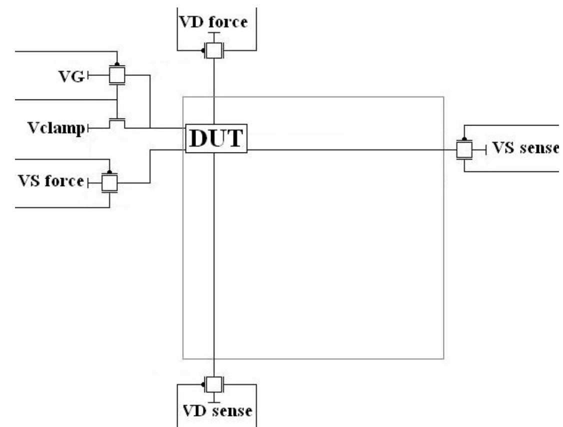

Figure 3(b) – DUT connection.

Using a row/column address decoders, only one transistor is selected. The other terminals of the non-selected transistors are clamped to their respective (N-Fet or P-Fet) clamp voltages to drive then in the accumulation regime. To drive current of the selected device to the measuring pin, transmission gates composed by thick oxide transistors (I/O transistors 2.5V) are used. The layout of the NMOS structure is shown in the figure 4. The entire layout of this structure including the PMOS and NMOS MOSFET Matrix, the bias circuitry, level shifters, address decoding and routing is shown in the Test Chip Overview section.

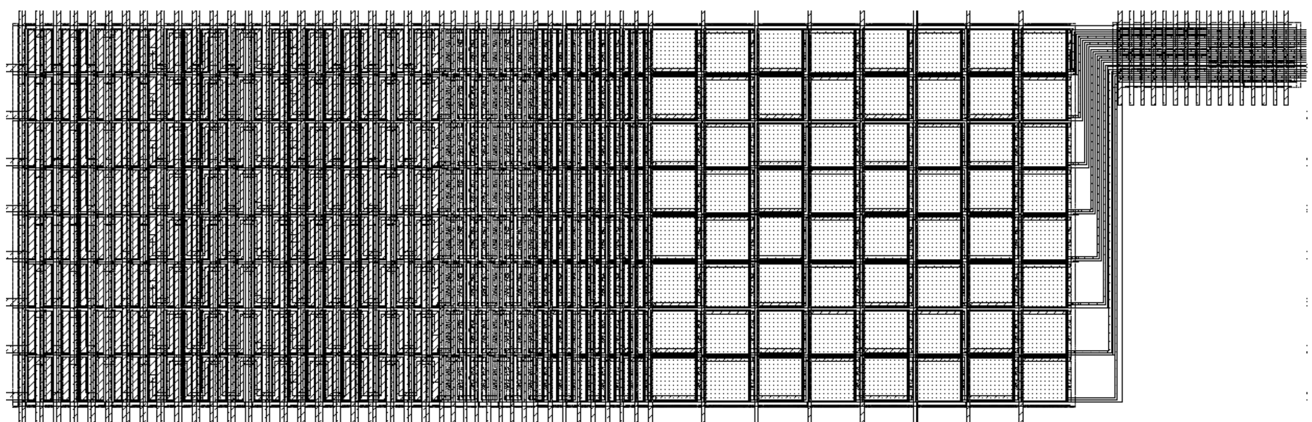

Figure 4 – MOSFET Matrix Layout.

3. MOSFET STACKED-PAIR MATRIX

The MOSFET stacked pair is composed of two identical MOSFETs connected in series, with their gate terminals in common as depicted in figure 5.

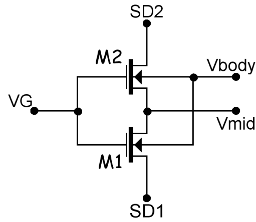

Figure 5 – MOSFET Stacked-Pair.

These two MOSFETs, namely M1 and M2, are nominally designed to be identical. However, various pieces of information can be obtained based on their differences (mismatch) just by measuring the middle voltage (V_{MID}) as a function of V_G. Hence, this circuit seems to be the most ideal and simplest structure suitable to monitor fabrication process [11-13]. It is possible to characterize transistor mismatch of a large set of devices in a small area. In this test chip we exercise two versions of measurement schemes for this circuit named Stacked-Pair Matrix.

3.1. Stacked-Pair Matrix Version 1

This version of the circuit is an array of the stacked pairs addressed by one decoder. The schematic diagram it is shown in the following figure 6.

During the measurement process, only one stacked pair is selected. The non-selected stacked-pair experience a clamp voltage VGS = Vclamp. For this version, as shown in figure 7, the layout of 64 minimum size pair transistors using 5 Metal levels is inserted in an 11 x 4 µm area. In the layout is shown that each transistor pair has its own gates connected, which is not the case of the next stacked pair version.

3.2. Stacked-Pair Matrix Version 2

The second version uses two decoders and allows to set up a stacked pair with the combination of transistors placed in different parts of the layout. The schematic diagram it is shown in the following figure 8.

This version connects externally the gate terminal (VG) and the measuring procedure is the as in version 1. The layout of 128 minimum size transistors (64 sharing the same active area) using 5 Metal levels is inserted in an 12 x 5 µm area as shown in figure 9. The entire layout of this structure is shown in the Test Chip Overview section.

4. STACKED-PAIR SIMULATIONS

As aforementioned, various pieces of information can be obtained based on M1/M2 differences depending on the applied bias condition.

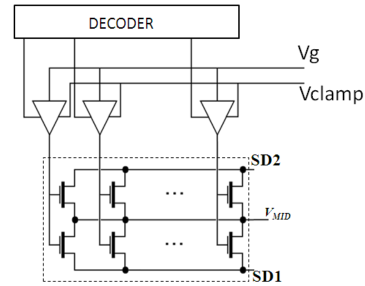

Figure 6 – Schematic stacked-pair matrix version 1.

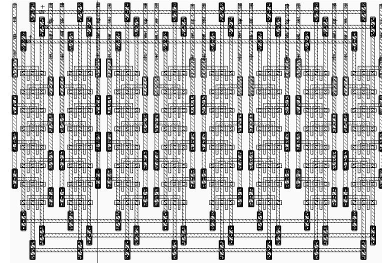

Figure 7 – Layout stacked-pair matrix version 1.

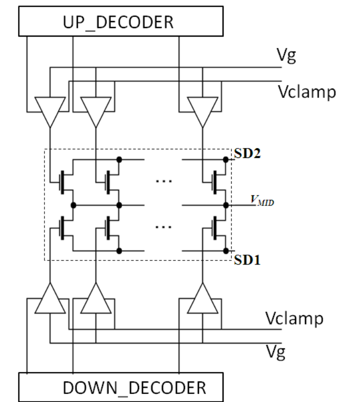

Figure 8 – Block diagram stacked-pair matrix version 2.

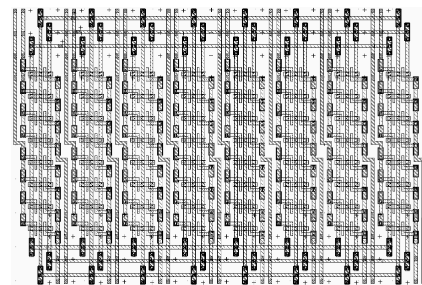

Figure 9 – Layout stacked-pair matrix version 2.

One measurement approach for this circuit is done in [12], which uses the V_{MID}^{ratio} vs. V_G characteristic. V_{MID}^{ratio} is the ratio of $V_{MID}^{forward}$ / $V_{MID}^{reverse}$. $V_{MID}^{forward}$ is the measured V_{MID} in the case where **SD1** = GND and **SD2** = VDD. $V_{MID}^{reverse}$ is the inverse of $V_{MID}^{forward}$, when **SD1** = VDD and **SD2** = GND. Therefore, as shown in [12], for a very low supply voltage, i.e. VDD = 100mV, several pieces of information can be extracted based on the differences between M1 and M2. In the next simulations, the V_{MID}^{ratio} vs. V_G behavior for stacked pair is shown for equal transistors with a controlled

perturbation on its parameters. The parameters are threshold voltage (V_{TH}) and channel length (L).

In figure 10 it is shown the V_{MID}^{ratio} vs. V_G characteristic for threshold voltage of transistor M1 (ΔV_{TH1}) decreased from default value 0V to -10mV.

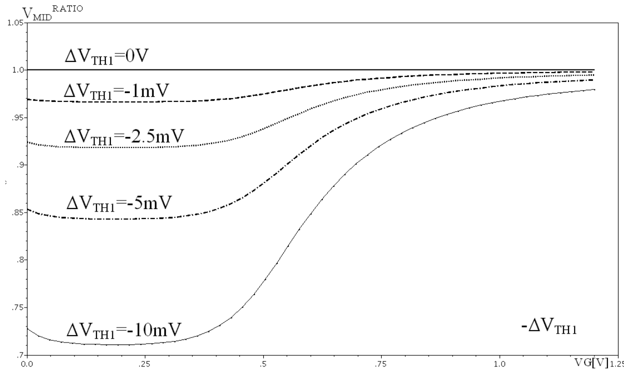

Figure 10 – V_{MID}^{ratio} versus V_G for $-\Delta V_{TH1}$.

In figure 11, the V_{MID}^{ratio} vs. V_G characteristic is plotted for channel length of transistor M1 decreased from L1 = 70nm to the default value L1 = 60nm (ΔL_1 = 10nm).

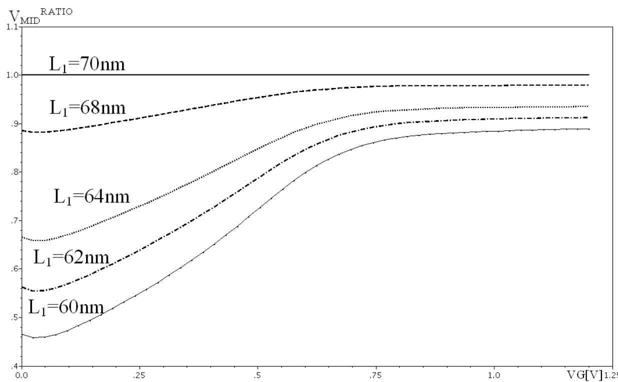

Figure 11 – V_{MID} ratio versus V_G -ΔL_1.

5. TEST CHIP OVERVIEW

Our test chip is shown in figure 12. The design size is 1.58 mm x 1.58 mm (with pads, without scribe lines), or 1mm x 1mm core size, under IBM 65 nm CMOS 10LPe/RFe design rules. An array of 44 Pads for packaging (OCP_LQFP44A by Mosis) is needed to access the internal test structures as previously described. Table I gives an overview of all blocks that compose the test chip, including the PADs, which were full custom designed in our group.

6. CONCLUSIONS

The test structures we developed for the local random variations characterization are composed of transistor arrays of identical size MOSFETs, and transistor pairs. Electrical measurements are indispensable for the complete validation of the test structures proposed in this chip. The measurements can be enabled in thousands of test transistors and pairs, using only 44 pads. They will be collected after MOSIS multi-project wafer fabrication is finished in a state-of-the-art commercial fab in 65 nm CMOS process.

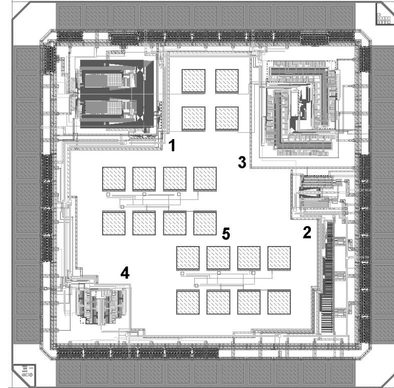

Figure 12 – Complete layout test chip.

TABLE I Chip Blocks.

#	Circuit	Area [µm x µm]
1	MOSFET Matrix	320 x 280
2	Ring Oscillators	200 x 480
3	Stacked-Pair Matrix version 1	390 x 320
4	Stacked-Pair Matrix version 2	205 x 155
5	µProbe Test Structures	2 x (930 x 280)

7. REFERENCES

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