

CMOS RECTIFIER USING THE COMPOSITE DIODE IN A BULK TECHNOLOGY

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ABSTRACT

This work presents the equationing of the conventional NMOS diode in the Weak Inversion regime to demonstrate that it has almost a diode behavior. To overcome the low forward to reverse current ratio of the conventional MOS diode, which cannot be acceptable in applications with low input voltage, it is presented the ULP Composite Diode developed by Levacq *et. al.* and it is equationed considering symmetrical PMOS and NMOS transistors in a BULK technology. The effect of the bulk connection in the reverse current is discussed and the simulations results are presented. The Cockcroft-Walton Multiplier is used to compare the performance of the NMOS diode and the ULP Composite Diode.

1. INTRODUCTION

Autonomous operating sensor system are getting very important in monitoring different physical parameters such as temperature, humidity, mechanical stress, etc. In many cases, the energy harvested by the converters circuits is too small, around a few mV [1], so that large voltage drop cannot be tolerated and thus common MOS diodes or even discrete Schottky must be avoided. MOS transistors can be used to replace them in order to safe area but it has a low forward to reverse current ratio which can be not acceptable in some applications. To handle with the reverse current issue, Levacq *et. al.* introduced in [2] a ULP Composite Diode which reduces the reverse current. Since the technology used in [2] is a Silicon on Isolator (SOI) there are some characteristics that is not achieved by a BULK technology like the slope factor close to 1. Thus this work presents the modeling of the MOS transistor diode connected and the ULP Composite Diode in a BULK technology.

The organization is the following: in part two the conventional NMOS transistor diode connected is modeled in Weak Inversion (W.I.) to demonstrate that in this region its behavior is almost the diode behavior. In part three the ULP Composite Diode is modeled also in W.I. region to prove that the reverse current is reduced and its bulk connection is discussed because the reverse current will depend on it. In part four, the Cockcroft-Walton Multiplier is used to compare the performance of the regular diode, the NMOS Diode and the ULP Composite Diode. Finally, in part five the conclusions are presented.

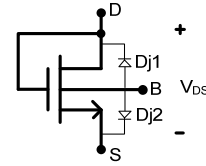


Figure 1 – NMOS Diode connected

2. CONVENTIONAL MOS DIODE

Diodes in MOS technology are usually implemented connecting the transistor as shown in Figure 1.

Although this configuration does not represent a physical diode, it can be demonstrated that if the transistor works in W.I. its $V \times I$ characteristic is close to the diode. There are two possible cases to be considered:

1) In a standard CMOS process the Bulk (B terminal in Figure 1) is connected to the ground, thus the channel current is given by:

$$I_{channel} = I_{SD} \left[\exp\left(\frac{V_D - nV_S}{n\phi_t}\right) - \exp\left(\frac{(1-n)V_D}{n\phi_t}\right) \right] \quad (2.1)$$

2) In a triple well technology, the Bulk can be connected to its source, thus the channel current becomes:

$$I_{channel} = I_{SD} \left[\exp\left(\frac{V_{DS}}{n\phi_t}\right) - \exp\left(\frac{(1-n)V_{DS}}{n\phi_t}\right) \right] \quad (2.2)$$

Where n is the slope factor, ϕ_t is the thermal voltage and:

$$I_{SD} = \mu_n \cdot C'_{ox} \cdot n \cdot \phi_t^2 \cdot e \cdot \frac{W}{L} \cdot \exp\left(\frac{-V_{T0}}{n\phi_t}\right) \quad (2.3)$$

is called saturation drain current which depends on the electron mobility (μ_n), the oxide capacitance per unit area (C'_{ox}), the threshold voltage (V_{T0}), and the aspect ratio (W/L). V_D is the voltage in the drain terminal (D), V_S the voltage in the source terminal (S) and V_{DS} is the difference between them.

3. ULP COMPOSITE DIODE

The drawback of use the NMOS diode connected is the junction parasitic diodes (D_{j1} and D_{j2} in Figure 1) which can be forward biased when the V_{DS} voltage is negative. To overcome this, Levacq *et. al.* presented the ULP composite diode topology in [2] which is shown in Figure 2.

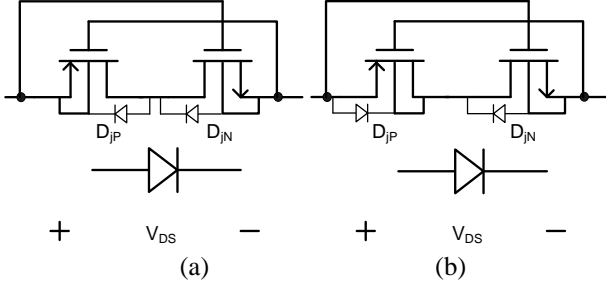


Figure 2 – ULP Composite Diode [2]

Assuming the transistor PMOS is symmetrical to the NMOS transistor (*i.e.* their threshold voltages are equal in module and they are sized to compensate the carrier mobility difference) the ULP Composite Diode current is given by:

$$I_{channel} = I_{SD} \cdot \left[\exp\left(\frac{V_{DS}}{n \cdot \phi_t}\right) - \exp\left(\frac{V_{DS} \cdot (2-n)}{2 \cdot n \cdot \phi_t}\right) \right] \quad (3.1)$$

It can be noted from Equation (3.1) that in the forward bias the second exponential term does not affect the current significantly. On the other hand, in the reverse bias both of them decrease rapidly instead of saturated in the saturation current of the diode (I_{SD}). The Figure 3(a) shows the comparison between the conventional NMOS diode with the ULP Composite Diode using equations (2.2) and (3.1) and in Figure 3(b) the curves extracted from the simulator with they sized in order to obtain a similar forward current.

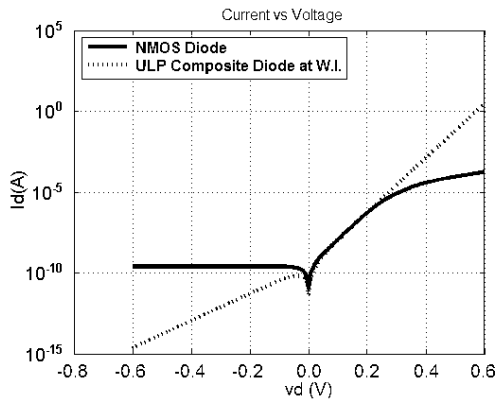


Figure 3(a) – I x V curve of NMOS diode and ULP Composite Diode

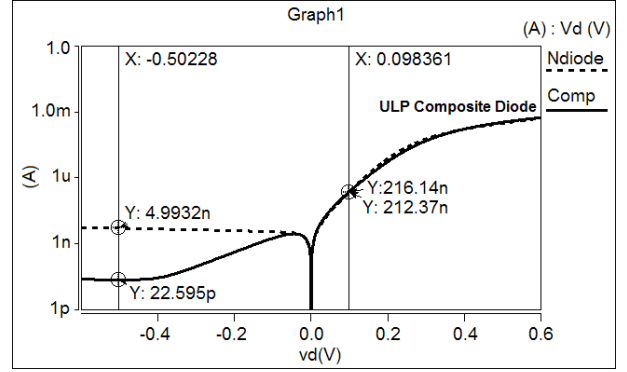


Figure 3(b) – I x V curve of NMOS diode and ULP Composite Diode extracted from simulator

In [2] the technology used was a fully-depleted SOI which does not have a bulk connection. If a BULK technology is used, the connection of the body terminal of the transistor PMOS has to be considered because it will affect the ULP Composite Diode current characteristic. If it is connected to the source, as shown in Figure 2(a), there are two junction diodes (D_{jp} and D_{jn}) forward biased for negative V_{DS} resulting in a rapid increase of the reverse current as shown in Figure 4(a). Otherwise, if the bulk is connected to the drain as shown in Figure 2(b) the junction diode (D_{jp}) will be reverse biased when V_{DS} is negative and thus limiting the ULP Composite Diode reverse current as can be seen in Figure 4(b).

4. VOLTAGE DOUBLER

An example of circuit which uses diodes is the voltage doubler shown in Figure 5.

At steady-state and disregarding the drops in the diodes, when the source is in the negative cycle, the capacitor $C1$ will be charged and the voltage across it will be equals to the peak of the input voltage. Thus in the next positive cycle the voltage across the capacitor $C2$ will be twice the peak of the input voltage.

The input voltage has 400mV of peak and frequency equals to 1kHz. The capacitance of capacitors $C1$ and $C2$ is 50pF.

The drop in the output voltage can be ascribed to parasitic capacitances, losses and the leakage current of diodes. As the capacitors used are much higher than the usually parasitic capacitances are, their effects can be disregarded. It can be noted from Figure 6 that the discharge of capacitor $C2$ is higher when NMOS Diodes are used due to their higher reverse currents and since the capability of provide forward current, and charge the capacitor, are in the same order for both NMOS Diode and ULP Composite Diode, a higher output level can be reached by the latter.

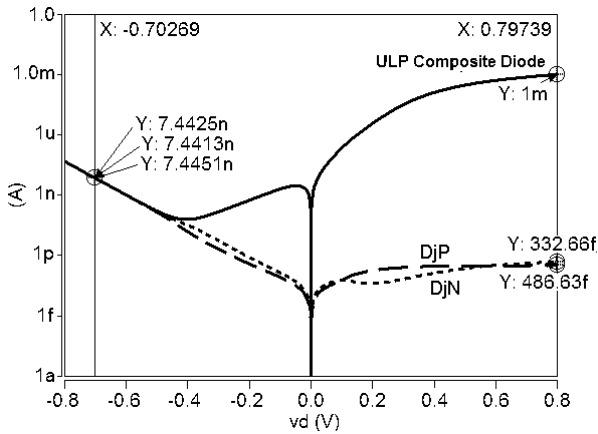


Figure 4(a) – Composite Diode current with the PMOS bulk connected to its source

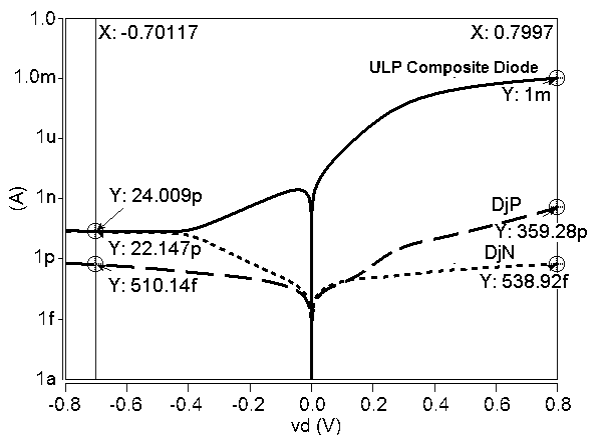


Figure 4(b) – Composite Diode current with PMOS bulk connected to its drain

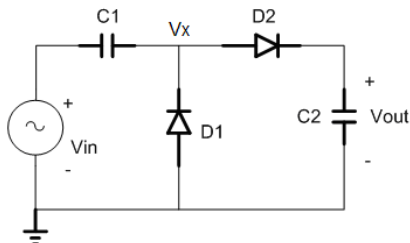


Figure 5 – Cockcroft-Walton Multiplier [3]

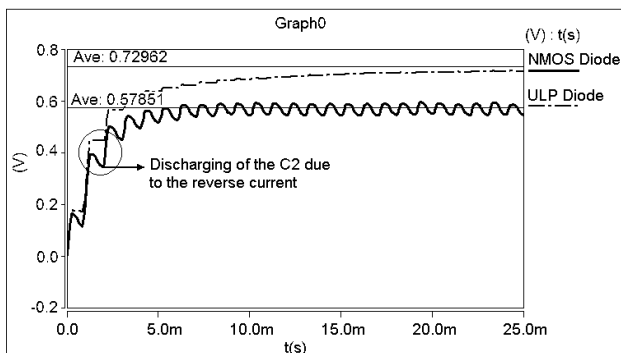


Figure 6 – Output voltage of Cockcroft-Walton Multiplier

5. CONCLUSIONS

It has been presented the transistor MOS operating as a diode. The modeling was made considering the operation in W.I. for the NMOS transistor diode connected and for the ULP Composite Diode. In the later, the total reverse current using the PMOS bulk connection in the drain demonstrate better results than connected to the source due to the junction diode. Using the ULP Composite Diode in the Cockcroft-Walton Multiplier the output voltage almost reaches its ideal value, *i.e.* twice the input voltage peak.

6. REFERENCES

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