ANALYSIS OF ELECTRICAL CHARACTERISTICS OF CARBON NANOTUBE ASSOCIATIONS OF TRANSISTORS AND COMPARISON WITH CMOS TECHNOLOGY

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ABSTRACT

This paper presents a study of the electrical characteristics of trapezoidal association of CNTFETs (Carbon Nanotube Field Effect Transistors). The goal is to perform an analysis between the CMOS technology and CNTFETs, both for 32nm node, and to verify the impact of new devices over electrical characteristics. We used for simulation predictive electrical models and we extracted the characteristic curves for large and small signals in both technologies. The simulation with CNTFETs was developed in Verilog-AMS, which is a high-level language for describing mixed circuits.

1. INTRODUCTION

Due to the necessity to reduce the size of transistors to supply the growing demand for integrated circuits with higher speed and lower power consumption, allied to the reaching of physical limits of silicon CMOS technology, it is mandatory to seek new alternatives for the miniaturization of devices. In order to provide electronics even faster, it is necessary to design transistors with large capacity to pass current. Thus, carbon nanotube transistors have great potential for replacing conventional semiconductor in microelectronics [1]. Despite the fact that the development of this technology is still in an early stage, CNTFETs serve to a variety of applications such as logic circuits, chemical sensors, RF circuits, etc. Figure 1 shows the structure of a CNTFET, consisting of four terminals (gate, drain, source and bulk), the same way as a CMOS transistor.

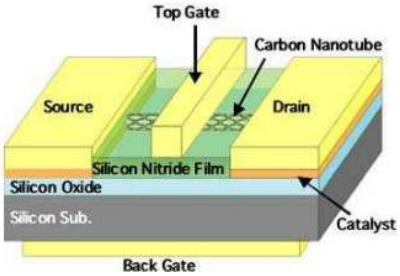

Figure 1 - Structure of a CNTFET

According to Figure 1 to allow for passage of current between the drain and source terminals, we must apply a voltage at the positive terminal of the gate (in the case of N-type transistors). Thus, the current flows towards the drain to source if voltage VDS is positive. It should be noticed that the speed of the CNTFET is higher in comparison with CMOS technology due to the fact that its channel consists of a tube of graphene with a small radius as small as 0.5nm in its cross section, as shown in Figure 2 [8].

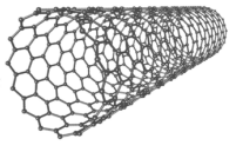

Figure 2 – A carbon nanotube.

This characteristic leads to the limitation that the channel width is not a free variable for the circuit designer, as it is for CMOS technology. A parallel association of nanotubes is necessary in order to provide a large channel width. Figure 3 shows the parallel association and the equivalence with CMOS technology.

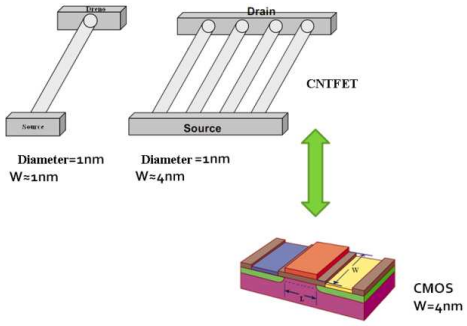

Figure 3 - Variation of channel width for CNTFET and CMOS technologies.

The characteristics of ballistic transport of carriers in the CNTFET result in higher intensity of electric current [3,4,5,6,7], which is an advantage over CMOS technology.

This paper presents an analysis of the electrical characteristics of series-parallel associations of carbon nanotube transistors and the comparison with the equivalent CMOS devices.

2. TRAPEZOIDAL ASSOCIATION OF TRANSISTORS (TATS)

The trapezoidal association of transistors (TATs), proposed by [9], is an alternative technique to assembly equivalent transistors composed by unit carbon nanotubes. It consists of two transistors in series, with the transistor connected to the drain terminal with a channel width (W) greater than the transistor connected to the source terminal. The channel length (L) of both transistors can be the same. The gates of the two

transistors are connected together, forming a device with the same characteristics of a single transistor. A trapezoidal association of transistors has as main characteristics a lower output conductance [9]. Figure 4 shows the geometry of a trapezoidal transistor.

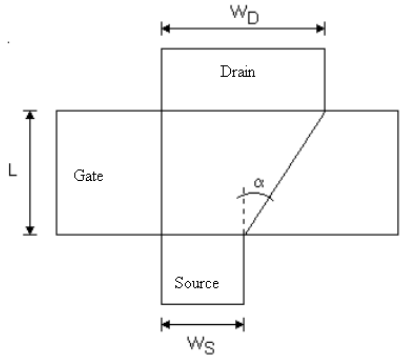

Figure 4 - Geometrical aspects of an intrinsic trapezoidal transistor [9].

The trapezoid format can be obtained by the proper composition of series-parallel unit transistors. Figure 5 shows how a trapezoidal association of transistors is assembled.

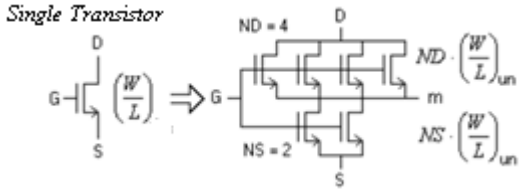

Figure 5 – Trapezoidal Association of Transistors.

For the trapezoidal format we must ensure that ND is larger than NS. ND is the number of unit transistors in parallel in the drain-end transistor and NS is the same for the source-end transistor.

3. COMPARISON BETWEEN CMOS AND CNTFET TRANSISTORS

For this work we used CMOS transistors with a channel width of 300nm and channel length of 32nm. For the CNTFET we used the same 32nm for the nanotube length, but we need to perform a calculation for estimating an equivalent parallel association in order to achieve the equivalence between the technologies. The diameter of a single nanotube can be estimated by following equation [3]:

$$D = a * s\sqrt{n1^2 + n2^2} + (n1 * n2)/\pi \quad (1)$$

The diameter is dependent on the way the carbon sheet is rolled up. The values of n1=19 and n2=0, informing that the nanotubes are rolled in zigzag type, give us a diameter of 1.5089nm . With this value, we estimated in 198 the number o nanotubes in parallel in order to achieve the channel width equivalence of 300nm. We call this a “set” of nanotubes. In order to make a comparison between CNTFET and CMOS technologies, we used predictive spice models (PTM) described in Verilog-AMS and simulated with HSPICE simulator. The CNTFET model is the Stanford PTM [3]. We performed electrical simulations for trapezoidal associations adopting ND=4 and NS=2. For this case, a CNTFET TAT is composed by 4 sets in parallel in the drain-end and 2 sets in parallel in the source-end. The curve IDS x VDS for both CMOS and CNTFET technologies is shown in Figure 6. Figure 7 shows the derivative of IDS x VDS, which results in the output conductance.

For generating the curve IDS x VGS we used the same parameters as previously, but maintaining VDS constant and varying the values of VG, as shown in Figure 8. The gate transconductance is shown in figure 9.

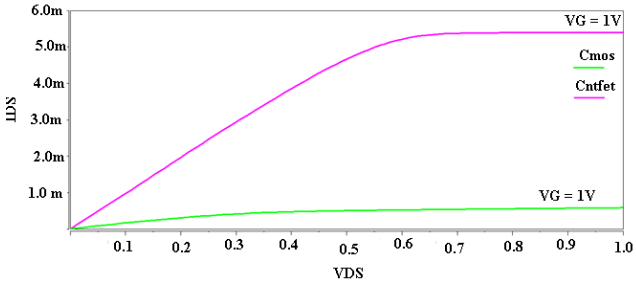

Figure 6 - IDS x VDS for CMOS and CNTFET.

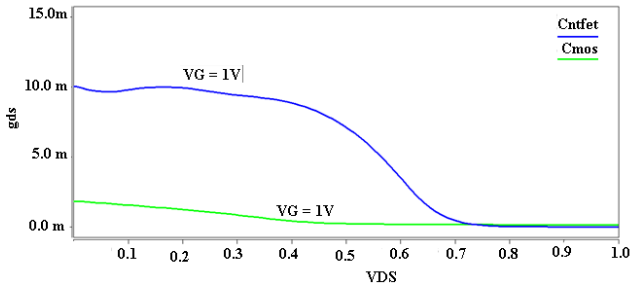

Figure 7 - gds x VDS for CMOS and CNTFET.

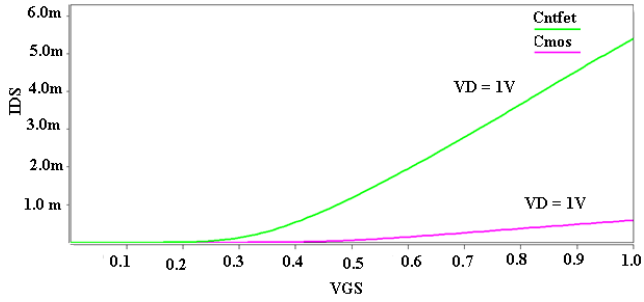

Figure 8- IDS x VGS for CMOS and CNTFET.

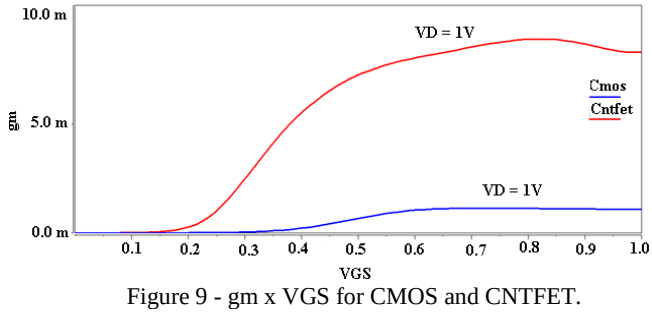

Figure 9 - gm x VGS for CMOS and CNTFET.

Based on the results above, we can see that the saturation current of the CNTFET for CMOS technology was

approximately 10 times higher than that of CMOS, as well as the CNTFET threshold voltage V_T was 0.3V and for CMOS technology it was 0.45V. This difference in technologies can be explained by the difference in the doping of the substrate. The output conductance gds and gate transconductance gm of the CNTFET are also larger than the CMOS, so it has a higher performance than conventional transistors, showing the quality of this device. After the analysis of a single CMOS transistor and an equivalent parallel association of nanotubes, we can explore simulations to verify the influence of ND and NS in a TAT association over the device large signal and small signal characteristics. First, setting ND in 10 and varying the value of NS from 1 to 9 we generated the curves shown in Figures 10(a-c).

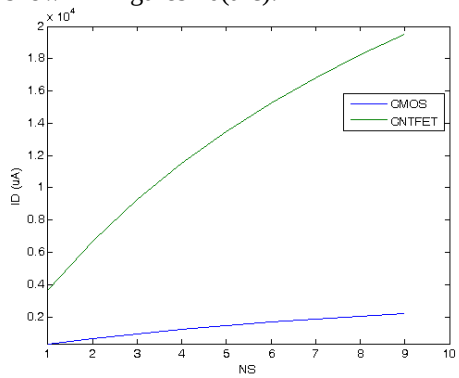

Fig. 10(a) - IDS x NS – CMOS and CNTFET

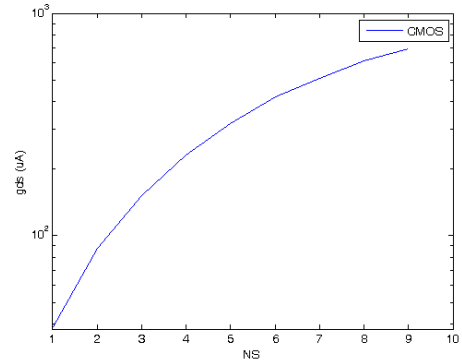

Fig. 10(b) - gds x NS – CMOS and CNTFET

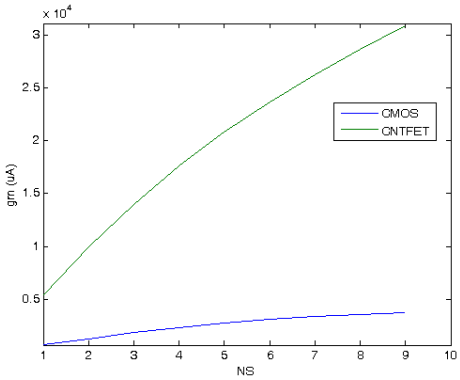

Fig. 10(c) gm x NS – CMOS and CNTFET

We can observe that the variation of the drain current in function of NS ranges from 400uA to 2200uA in the CMOS device, while the CNTFET device provided 4000uA to 19000uA. The CMOS output conductance increases with the variation of NS. In the CNTFET we observed that the output conductance related to NS was practically zero. The variation of the gate transcoductance in relation to NS increased from 500uA/V to 3900uA/V in the CMOS version, while in CNTFET version the gate transconductance increased from 5000uA/V to 31000uA/V. Based on the electrical simulations we can see that the CNTFET trapezoidal association achieves a larger drain current. This fact can be explained by the ballistic transport nature of the carbon nanotubes. Varying the ND from 2 to 10 and fixing NS=1 for both technologies, we generated the curves shown in figure 11(a-c).

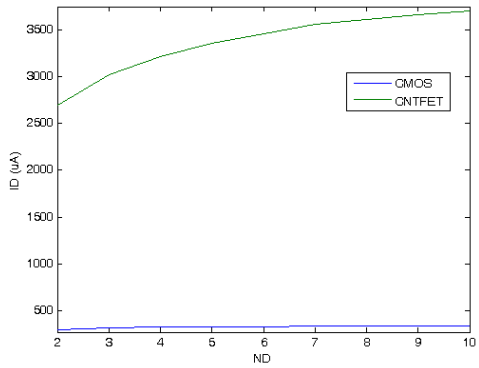

Fig. 11(a) - IDS x ND – CMOS and CNTFET

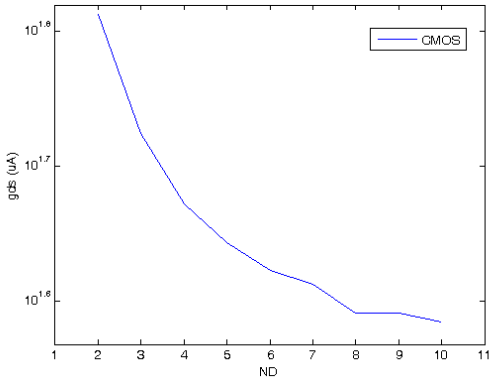

Fig. 11(b) - gds x ND – CMOS and CNTFET

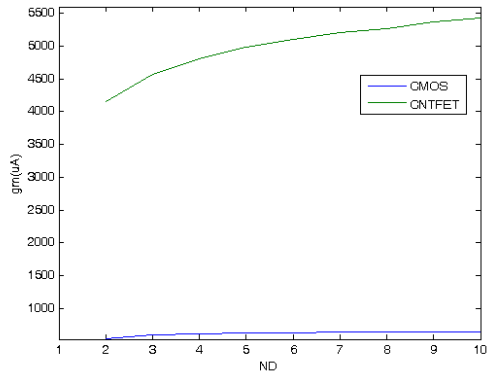

Fig. 11 (c) - gm x ND – CMOS and CNTFET

We can notice that the variation of the drain current in the CMOS device related to ND increased from 293uA to 338uA, while the variation of the drain current in the CNTFET increased from 2700uA to 3600uA. In 11(b)

the CMOS output conductance decreases with the increase of ND. For the CNTFET we observed that the value of the output conductance was virtually zero in the saturation region. The gate transconductance increased in the CNTFET from 4100uA/V to 5400uA/V, and from 540uA/V to 640uA/V in the CMOS.

The electrical characteristics of trapezoidal associations of CNTFETS are similar to that of CMOS, providing better gm/gds ratio for higher ND/NS.

4. CURRENT MIRROR

In order to verify the improvement in output conductance caused by the trapezoidal arrangement, we simulated a current mirror circuit in both CMOS and CNTFET technologies. Electrical simulations were performed on both technologies, according to the schematics of fig. 12. The simulations were performed with Synopsys HSPICE. Figure 13 shows the resulting output current in relation to the variation of the load.

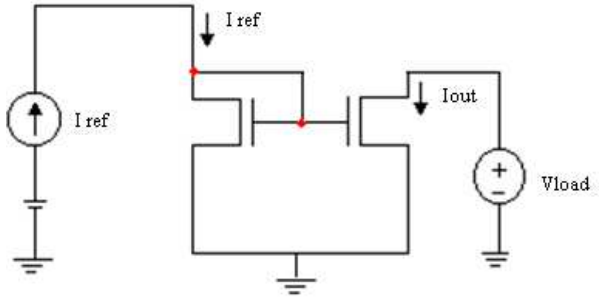

Figure 12 – Schematics of the simulated current mirror.

Analyzing these curves we can see that CNTFET technology presents better results compared to the CMOS technology. The advantages of the use of CNTFETs can be summarized as the fact that it reaches the saturation in a load voltage smaller than CMOS and also that the reference current benefits from the lower output conductance.

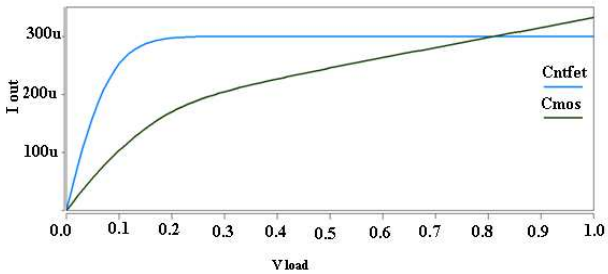

Figure 13 – I_{out} versus V_{load} for CMOS and CNTFET current mirror.

5. CONCLUSION

This paper presented an analysis and comparison of CMOS technologies and CNTFET. Based on the results we can observe that CNTFETs are promising to replace conventional transistors in some applications, mainly because they have some better electrical characteristics than the CMOS. The trapezoidal association of carbon nanotubes is a good alternative for the generation of high performance analog basic circuits. The challenge is to produce nanotubes on a commercial scale with reliability and productivity comparable to CMOS technology, a fact that is not yet possible because of the great variability and instability in the manufacturing process.

6. REFERENCES

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