GM/ID METHODOLOGY USING EVOLUTIONARY ALGORITHMS AND ELECTRICAL SIMULATION FOR INTEGRATED CMOS OTA DESIGN AUTOMATION

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ABSTRACT

The goal of this paper is to analyze the gm/I_D methodology for automatic sizing of analog integrated amplifiers. This methodology exploits the analytical gm/ID methodology, in which the inversion level of the transistors are free variables and gate width and length are defined in terms of the technology independent gm/ID versus ID/(W/L) curve. Genetic Algorithms was used as optimization heuristic together with a Spice simulator for implementing a power-constrained design of a two-stage Miller operational transconductance amplifier for different gain-bandwidth requirements.

1. INTRODUCTION

The design automation of analog integrated circuits is a demanding task in microelectronics industry, because of the crescent necessity for low-power design and reduced time-to-market. Nowadays, most analog sizing designs are done manually – with some aid of simulation tools and equation-based models - and the quality of the resulting circuit is dependent on the expertise of the designer. For example, a system-on-chip (SOC) design can have analog and digital parts, each one designed with different methodology and tools. The analog design time must be compatible with the highly automated digital design time, which employs advanced design automation tools [1]. Also, in general the entire design space exploration is rarely executed, mainly in weak and moderate inversion regions, which are the most appropriated for power-constrained applications.

The design of analog integrated circuits can be divided in 3 steps: topology selection, transistor sizing and layout generation. This paper will focus on the second step, which is critical for achieving the desired circuit performance under a set of constraints.

The design space for the automatic synthesis of an analog CMOS integrated amplifiers is highly nonlinear. There are about ten free variables in a typical operational transconductance amplifier design, related to gate dimensions (W and L), bias currents or inversion levels. As the relation between transistor sizes and circuit specifications (design objectives) is nonlinear and sometimes conflicting, the problem of finding an optimum solution point is difficult to be exactly solvable and it usually must be approximated by analytical or numeric analysis. Some previous works have been done in this theme describing the development of tools for analog design automation (ADA). The goal is always the automation of time-consuming tasks and complex searches in highly non-linear design spaces [2][3][4]. Different automatic design strategies have been proposed, using different meta-heuristics and algorithms [5][6]. Basically all of them can be categorized as equation-based or simulation-based automatic designs. In the equation-based design strategy, analytical equations are used for modeling device electrical characteristics, such as drain current, inversion level or small-signal parameters. These models are often simplified or manipulated in order to fit certain limitations imposed by optimization heuristics. The simulation-based strategy is based on the result of the electrical simulation of the circuit to extract device parameters and design characteristics. The simulation can be automated and performed several times until reaching the design objective.

The goal of this paper is to analyze a technique for automatic sizing of analog integrated amplifiers that exploits the analytical gm/ID methodology, in which the transconductance (gm) to drain current (ID) ratio of the transistors are free variables and gate width and length are defined in terms of the technology independent gm/ID versus ID/(W/L) curve. We used in this work an evolutionary heuristic for finding a close to optimum solution. Circuit specifications are evaluated using an external electrical simulator.

As design example we show the sizing procedure of a power-constrained design of a two-stage Miller operational transconductance amplifier for different gain-bandwidth requirements.

2. EVOLUTIONARY HEURISTICS

In this implementation, it was used an evolutionary heuristic named Genetic Algorithms (GA) for generating the optimized sizes for the transistors of an analog circuit.

Evolutionary heuristics are very useful in non-linear optimizations and large design space exploration. They start from a random initial solution and the optimization process is performed with several solutions in parallel (population).

In GA, there are two main parameters: the chromosome (a solution candidate for the problem) and the population (a set of chromosomes).

New solutions are generated using the solutions present in the population and the generation of new solutions is implemented using the Crossover and Mutation parameters.

An important choice in an optimization using GA is the number of individuals in the population, because the GA deals with several solutions simultaneously. A large population increases the diversity of solutions but also increases the optimization time. Then, the number of population individuals must be chosen according to criteria of assuring solution diversity but maintaining a practical optimization time.

In this paper we used the implementation GAOT (Genetic Algorithms Optimization Toolbox) for Matlab [7].

3. GM/ID METHODOLOGY

In the design procedure herein proposed, a methodology called g_m/I_D is used for the circuit performance evaluation. This methodology considers the relationship between the ratio of the transconductance g_m over DC drain current I_D and the normalized drain current $I_n = I_D/(W/L)$ as a fundamental design parameter [8], such as the curve shown in Figure 1. The g_m/I_D characteristic is directly related to the performance of the transistors, gives a clear indication of the device operation region and provides a way for straightforward estimation of transistors dimensions.

The main advantage of this method is that the g_m/I_D x I_n curve is unique for a given technology, reducing the number of electrical parameters related to the fabrication process. Additionally, its analytical form covers all transistor operation regimes, from weak to moderate to strong inversion. The g_m/I_D x I_n curve can be automatically evaluated by electrical simulation or by measurement data.

Figure 2 shows the proposed optimization design flow using Genetic Algorithms. The user enters the design specifications, technology parameters and configures the cost function according to the required design objectives and specifications.

The optimization loop performs a random perturbation on the design variables, defined by the genetic algorithms. These variables are defined by the user, and are always related to the transistor geometry, large and small-signal parameters, such as W, L, I_D, g_m and g_m/I_D. So using the gm/ID x IN curve and the specifications required for circuit the transistor sizes are find. If the circuit is feasible, i.e., transistor sizes are within an allowed range, the circuit specifications can be evaluated using the electrical simulations and the solution is evaluated using the cost function. While the stop conditions are not satisfied are generated new solutions.

In GA are typical stop conditions: the maximum number of generations and the minimum variation in the cost function.

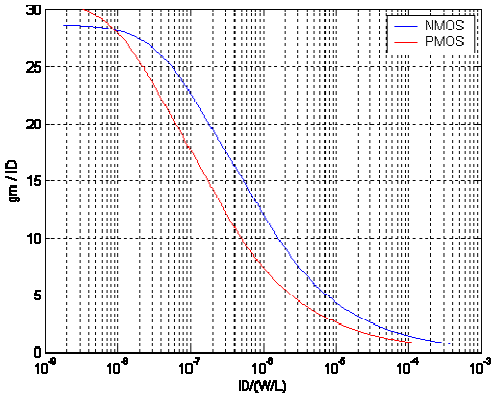

Figure 1: *gm/I$_D$* x *I$_D$/(W/L)* curve for NMOS and PMOS, 0.35µm CMOS technology.

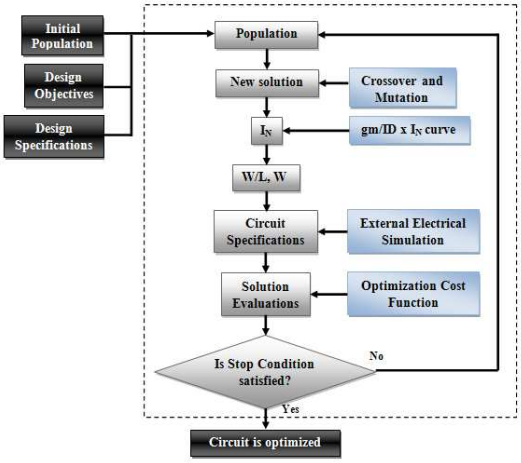

Figure 2: Design flow for the gm/I$_D$ design methodology

4. DESIGN EXAMPLE AND ANALYSIS OF OPTIMIZATION RESULTS

As a design example using the design methodology described in this paper, we used a two-stage CMOS Miller operational transconductance amplifier (OTA). The circuit schematic of this amplifier is shown in Figure 3. The Miller OTA is composed by an input differential pair and a current mirror with active load in the first stage. The second stage is composed by an inverter amplifier. Between the first and second stages is connected a compensation capacitor for stability purposes.

The main specifications of this circuit are low frequency gain (Av), slew rate (SR), margin phase, input common-mode range (IMCR), power consumption and gate area [9].

The optimization strategy relies on minimizing a cost function, given as

$$f_c = \sum_{i=1}^{n} \alpha_i \hat{p}_i(X) + \sum_{j=1}^{m} \beta_j \hat{c}_j(X) \quad (1)$$

where α_i is the weighting coefficient for performance parameter $\hat{p}_i$, which is a normalized function of the vector of independent design parameters X (free

variables). This function allows the designer to set the relative importance of competing performance parameters, such as, for example, a weighted relation between power and area. The parameter $\hat{c}_j(X)$ is a constraint normalized function, which limits the design space to feasible solutions of design specifications.

The coefficient β_j indicates how closely the specification must be pursued. If $\hat{c}_j(X)$ is inside a given specification, i.e. the value is major that the minimum and smaller than a percentage of minimum value, it is set to zero.

The cost function is computed at every iteration in the optimization loop. The correct design space exploration is directly related to the cost function formulation [7][8].

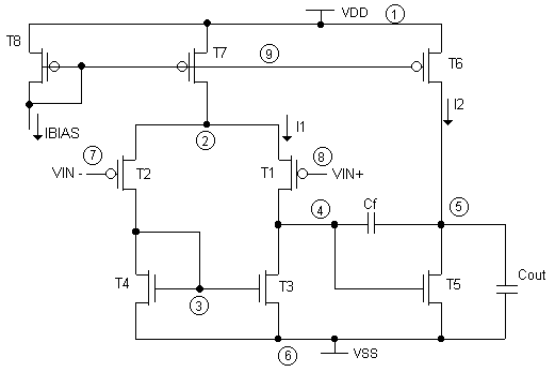

Figure 3: Schematics of a two-stage Miller operational transconductance amplifier

For this design example we implemented three different designs specifications aiming to the minimization of the gate area and the power consumption of the circuit.

For the Genetic Algorithm configurations we used a population of 1000 individuals. The results of the three designs are shown in Tables 1, 2 and 3.

Analyzing the optimization results we observe that all specifications are reached in the three designs. We can notice that the major part of the designed values are kept in a maximum of ten percent of the minimum values of the specifications. In the first design the power consumption is very low as expected, due to the unity frequency and slew-rate requirements.

Figures 4, 5 and 6 show the cost function value of the best solution during the optimization. In this figure we can see that the values of this function start from a high value and finish in a lower value, showing the optimization path in the cost function value.

Tab. 1: Specifications and reached values for the design 1.

Parameter	Spec.	gm/ID M.
Av0 [dB]	≥ 70	73.50
GBW [MHz]	≥ 0.1	0.1
Phase margin [°]	≥ 60.0	63
Slew rate [V/µs]	≥ 0.1	0.1
ICMR+ [V]	≥ 0.7	1.3
ICMR- [V]	≤-0.7	-1.64
Power consumption [µW]	minimize	3.52
Gate area [µm²]	minimize	740.80

Tab. 2: Specifications and reached values for the design 2.

Parameter	Spec.	gm/ID M.
Av0 [dB]	≥ 70	70.10
GBW [MHz]	≥ 1	1.0
Phase margin [°]	≥ 60.0	60.8
Slew rate [V/µs]	≥ 1	0.99
ICMR+ [V]	≥ 0.7	1.35
ICMR- [V]	≤-0.7	-1.60
Power consumption [µW]	minimize	58.20
Gate area [µm²]	minimize	502.46

Tab. 3: Specifications and reached values for the design 3.

Parameter	Spec.	gm/ID M.
Av0 [dB]	≥ 70	76.00
GBW [MHz]	≥ 10	10.00
Phase margin [°]	≥ 60.0	98.1
Slew rate [V/µs]	≥ 10	9.9
ICMR+ [V]	≥ 0.7	1.31
ICMR- [V]	≤-0.7	-1.64
Power consumption [µW]	minimize	296.01
Gate area [µm²]	minimize	6678,26

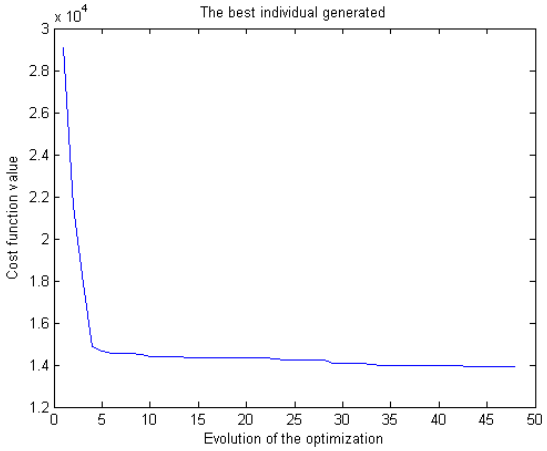

Fig. 4: Cost function value of the best solution during the optimization of design 1.

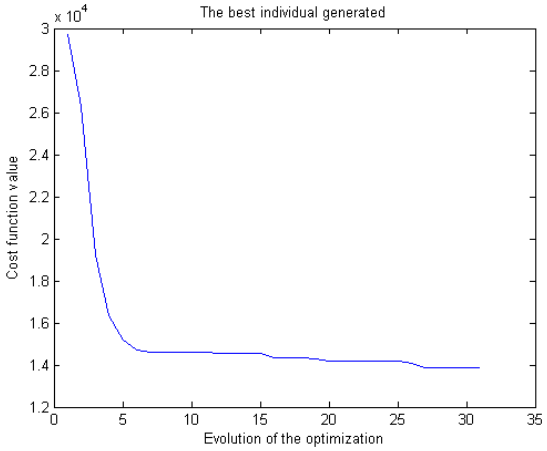

Figure 5: Cost function value of the best solution during the optimization of design 2.

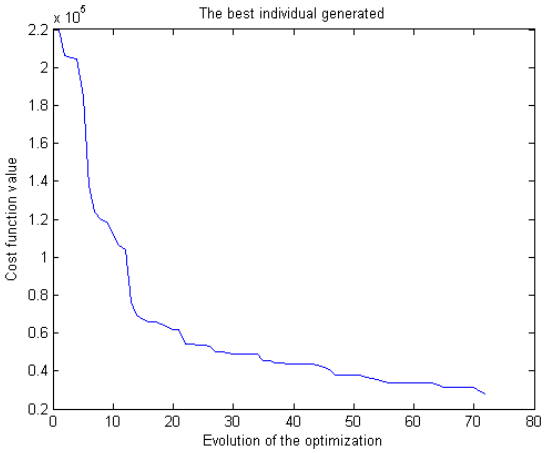

Figure 6: Cost function value of the best solution during the optimization of design 3.

6. CONCLUSION

In this paper an automatic gm/ID methodology using genetic algorithms and electrical simulation was implemented.

As design example a two-stage Miller OTA was automatic designed for three different specifications. In those designs all specifications were reached and the power consumption and gate area were optimized. The major part of the optimized values are kept in a maximum of ten percent of the minimum values of the specifications. As future work we intend to make a comparison to other methodologies, insert the analysis of parameter variations, and expand the methodology for other analog circuits.

7. ACKNOWLEDGMENTS

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