DEVELOPMENT OF HARDWARE AND SOFTWARE COMPONENTS FOR A PLATFORM FOR NOC EVALUATION IN FPGA

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ABSTRACT

In order to explore the design space of Networks-on-Chip and evaluate the impact of different network configurations on the system performance, designers use simulation based on different abstraction levels. This paper presents the development of hardware and software components for platform for assessing a direct emulation of a NoC in FPGA, allowing for real-time evaluation of the network performance.

1. INTRODUCTION

The Network-on-Chip (NoC) approach [1] has emerged as a solution for the problem of interconnecting cores in future Systems-on-Chip (SoC) with from dozens to hundreds of cores integrated on a single chip.

Several research groups have investigated different issues about Networks-on-Chip (NoCs), and most of them use simulation environments to evaluate the performance of their proposals, as done by [2] and [3].

Depending on the abstraction level used to model the NoC and the system components, the computational cost of simulation may become impracticable, limiting the system size and simulated time.

An alternative is the use of synthesizable models of networks and traffic generators (which emulate the traffic generated by components of real systems) which allow to carry out to network performance evaluation on FPGA (Field Programmable Gate Array). This approach provides a significant gain in the evaluation because it allows the execution of a greater number of operation cycles of the network in the same experiment time compared to simulation. Moreover, as the evaluation is done on the synthesizable model, this type of experiment allows the network physical validation.

The following text is organized in four sections, including a discussion about related works, issues regarding development and validation, and the conclusions.

2. RELATED WORKS

In [4], it is presented an environment for performance evaluation of a NoC based on hardware-software emulation, being able to compare many models of NoC architectures at the physical level through experiments conducted with the implemented NoC directly in hardware. The approach used allowed to speed up the performance evaluation by about four orders of magnitude when comparing to an approach based on simulation at RT level. According to the authors, an experiment involving the transfer of one billion of packets consumes less than four minutes in the emulation environment, and the SystemC RTL simulation of the same experiment spends about six days. This can be explained by the fact that in the simulation, each component (routers, traffic generators and traffic receptors) is simulated through blocks of code executed sequentially on a single processor. In emulation, all of these components are "run" in parallel because they are physically synthesized on a chip.

In [5], the Authors obtained lower gains (80-300 times) when compared with SystemC simulation. However, in this approach, the authors proposed a sequential emulation in a single router which is implemented in FPGA. The platform emulates larger networks running sequentially. The advantage in this case is to allow the emulation of networks of any size.

3. DEVELOPMENT

This work aims at developing a platform for performance evaluation of SoCIN (SoC Interconnection Network) [6] directly on FPGA. The platform consists of hardware and software components. The hardware components are integrated into a SoC composed of instances of the ParIS router (Parameterizable Interconnect Switch) [7], cores for traffic generation (TG) and traffic measurement (TM), and a module for communication and control (CCM). The platform, depicted in Figure 1, also includes a software running on a computer, which is called Supervisor. This software is responsible for the tasks of setting up the TGs with the traffic to be generated, collecting data from the TMs and analyzing the result. It communicates with CCM by using a communication driver and an RS-232 cable.

The implementation of the TG and TM cores is described in [8]. They are singe purpose processors implemented as configurable cores designed to generate traffic and collect performance metrics with minimal latency.

The CCM block was implemented in the context of this work. It is composed by a Xilinx MicroBlaze

processor, which is interconnected to a UART and a specific peripheral through PLB (Processor Local Bus). target computer, a RS-232 terminal was executed to receive and display the transferred data.

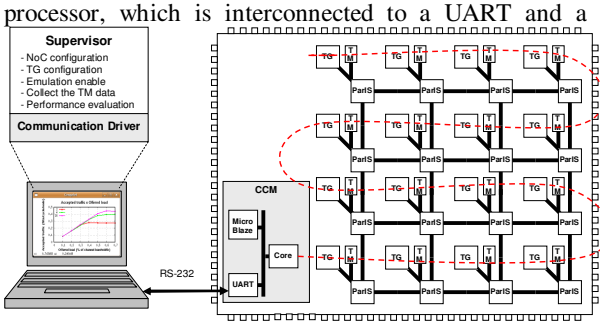

Figure 1 – Platform for performance evaluation of NoC

The Supervisor software was designed to be integrated into the BrownPepper tool [9], which consists of an integrated performance evaluation of NoC based on SystemC simulation. BrownPepper includes a set of tools that automates many tasks necessary for the exploration of the design space of NoC projects.

Figure 2 illustrates the design flow that integrates the Supervisor software with the BrownPepper tool and the RS-232 interface (UART). Initially, the supervisor reads the *traffic.tcf* file (1) and generates the intermediate file named *traffic.mif*. After that, in (2), the Supervisor generates the *traffic.bst* file, which finally (3) is transferred to the CCM block, in the FPGA, through the RS-232 interface.

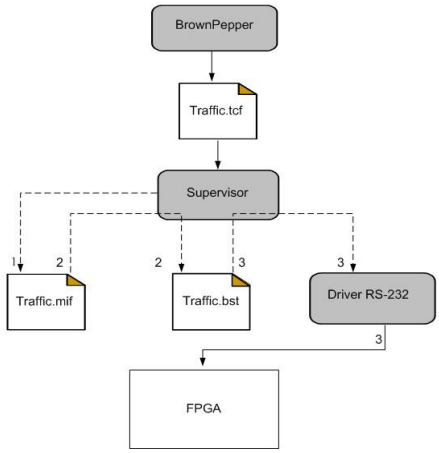

Figure 2 – Design flow

4. RESULTS

4.1. Driver Validation

In order to validate and verify the correctness of the data transmitted by the algorithm after the bitstream creation, a test environment was developed using the RS-232 ports from two different computers and connected via a serial communication cable. On the source computer, the Supervisor software read a *traffic.tcf* file and the generated bitstream was sent to the target computer through the RS-232 interface. On the

4.2. CCM Validation

The validation of the CCM in the FPGA was done by using the Digilent NEXYS 2 FPGA development kit. This kit has the required devices for the development of this work, including a Xilinx Spartan 3 1200-E FPGA and an RS-232 port, besides other devices. In the validation experiments, the Supervisor sent streams of bytes though the RS-232 port, which was received by the CCM and presented on a set of LEDs available on the kit.

5. CONCLUSION

This paper presented the architecture of a platform for performance evaluation of a NoC directly on FPGA. The paper described the architecture and functionality of a set of hardware and software components (CCM and Supervisor) which was developed to be used with previously implemented components (ParIS, TG, TM and BrownPepper). This is an ongoing work and future tasks includes the integration of all the components and a set of experiments to evaluate the correctness and effectiveness of the proposed platform.

6. ACKNOWLEDGMENTS

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