Analysis of Optimization Techniques For Fully Integrated 915MHz CMOS LNA Design

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ABSTRACT

This paper presents an investigation of noise figure optimization techniques for a 915 MHz CMOS Low Noise Amplifier (LNA). The research's goal is to evaluate the trade off between fully and partially integrated solutions for 915 MHz CMOS LNA. The analysis considers an inductively source-degenerated cascode topology, which is capable of achieving simultaneous noise and input match, with narrow band-width and low power. Two different circuits were designed in 0.35μm CMOS technology with a supply voltage of 1.8V to evaluate the fully and partially integrated version. A noise figure of 2.97dB, gain of 11.37dB, IIP3 of 3.67dBm with 12.67mW of power dissipation were obtained through simulations for the fully integrated version, while the partially integrated one got 1.37dB, 10.11dB, -8.27dBm for the same parameters with only 2.67mW of power consumption.

1. INTRODUCTION

A RF receiver overall sensitivity is dominated by the LNA gain and noise figure, which turns the LNA into the most delicate block in a receiver system. For narrowband system, such as sensor networks, the inductively source-degenerated topology is the most adopted one for LNAs, due to it ability to simultaneously match noise and input impedance. Several design techniques has been proposed for this topology, considering the noise figure optimization for acceptable gain and power consumption.

Nguyen et al. [1] revised a set of four LNA design technique and demonstrated a power-constrained methodology with simultaneous noise and impedance matching. The method, however, achieve the optimum noise figure only for large gate inductor values and neglecting its noise contribution due to its parasitic resistance.

Belostotski and Hasllet [2] evaluated the impact of the integrated gate inductor's quality factor on the noise performance of inductively source-degenerated LNAs. Their paper proposed a power-constrained noise optimization with minimum gate inductance method, as a sub-case of the optimization technique under power and gain constraint. The approach used considers the use of wire bond inductors with high quality factor, which minimize its parasitic noise, which works at 2.5 GHz. However, at lower frequencies such as 915 MHz, the value of gate inductors are too big to be implemented with wire bonds [3].

The methodology section of this paper presents a review of LNA theory and modifications on Belostotski and Hasllet's technique. The feasibility section analyzes the loss and gains on operation frequency decreasing and technology scaling down. The results section shows two designed LNAs to evaluate the trade off between integrating the gate inductor or placing it off-chip. The conclusion shows that integrating this inductor demands a large increase of power consumption, yet achieving worse noise factor.

2. METHODOLOGY

In order to optimize the LNA parameters, it is necessary to obtain their expressions, for the chosen topology. In this case, an inductively source-degenerated cascode architecture was selected, as shown in Figure 1, due to its ability to simultaneous match noise and input impedance, with narrow gain, for low consumption levels [1].

The noise factor expression was evaluated taking into account the thermal noise contribution from parasitic resistance attributable to gate inductor (Lg) and transistor gate, the traditional thermal channel noise and induced gate noise sources and neglecting the gate-drain parasitic capacitance in M1, the noise contribution of the cascode transistor M2 and the noise contribution due to the Ls parasitic series resistance.

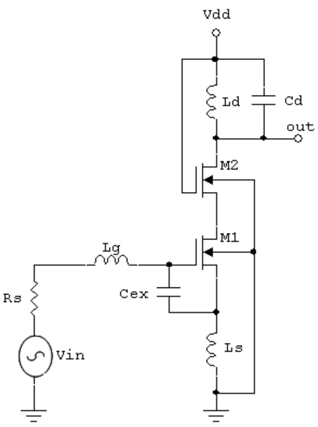

Figure 1. Inductively source-degenerated cascode adopted topology.

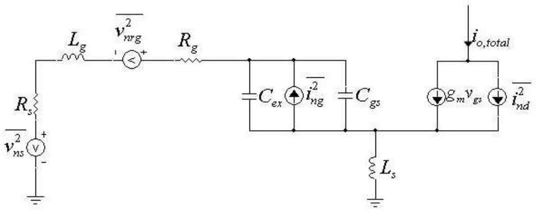

Figure 2. Small-signal model used to derive noise figure expression.

These assumptions were made in order to simplify the calculus, knowing they introduce small error in the LNA input impedance and noise figure 2.

The noise figure for the circuit shown in figure 2 (equation 2), can be derived replacing the expressions for the output noise current due to each noise source alone (where iout1 is associated with the source resistance) on equation (1) and noticing that the only two correlated noise source are i_{ng}^2 and i_{nd}^2. The detailed derivation of this noise factor can founded on Belostotski and Hasllet work [2].

$$F = \frac{\left|i_{o,total}\right|^2}{\left|i_{out1}\right|^2} = \frac{\left|i_{out1} + i_{out2} + i_{out3} + i_{out4}\right|^2}{\left|i_{out1}\right|^2} \qquad (1)$$

$$F = \frac{R_s + R_g}{R_s}\left\{1 + \frac{\left(C_{gs} + C_{ex}\right)^2}{C_{gs}^2}\frac{R_s + R_g}{R_s}\frac{\omega^2 R_s C_{gs}^2 \gamma}{\alpha g_m}\left[\frac{\delta\alpha^2}{5\gamma}\left(Q_s^2 + 1\right)\frac{C_{gs}^2}{C_t^2} + 1 - 2|c|\frac{C_{gs}}{C_t}\sqrt{\frac{\delta}{5\gamma}}\right]\right\} \qquad (2)$$

Considering equation 2 and input matching, the expressions for the amplifier transconductance and noise figure can be obtained after some calculation, as can be seen in appendix II of Belostotski and Hasllet work [2]. These expressions are re-presented here by equation (3) and (4) in function of the overdrive voltage v_{od} and the additional gate-source capacitance C_{ex}. The independent terms are chosen for being easily controllable at design.

$$G_m(v_{od}, C_{ex}) = \frac{gm(v_{od})}{2R_S\omega\left(C_{ex} + C_{gs}\right)\left(v_{od}, C_{ex}\right)} \qquad (3)$$

$$F(v_{od}, C_{ex}) = \frac{R_s + R_g(v_{od}, C_{ex})}{R_s}\left\{1 + \frac{R_s + R_g(v_{od}, C_{ex})}{R_s}\frac{\omega^2 C_t(v_{od}, C_{ex})^2\gamma}{\alpha(v_{od})g_m(v_{od})}\chi\left(v_{od}, C_{ex}\right)\right\} \qquad (4)$$

where,

$$\chi\left(v_{od}, C_{ex}\right) = \frac{\delta\alpha(v_{od})^2}{5\gamma}\left(Q_s^2 + 1\right)\frac{C_{gst}(v_{od}, C_{ex})^2}{C_t^2(v_{od}, C_{ex})} + 1 - 2|c|\frac{C_{gs}(v_{od}, C_{ex})}{C_t(v_{od}, C_{ex})}\sqrt{\frac{\delta}{5\gamma}}$$

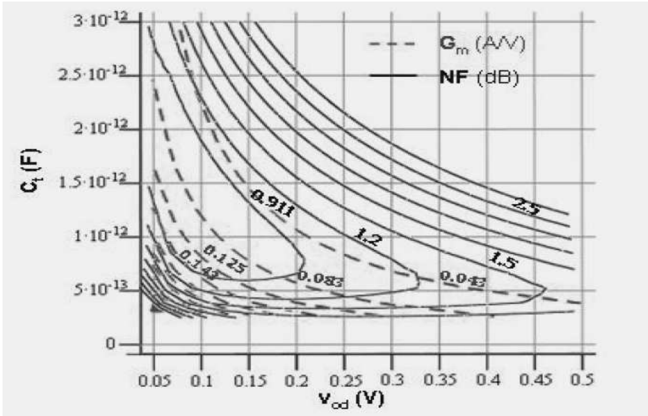

Figure 3. Overlaid plots of noise figure and tranconductance (gain) for constante power consumption. Parameter used were: $\gamma = 2/3$, $\delta = 4/3$, $c = j0.395$, $E_{sat} = 4.7\cdot10^6$ V/m, $v_{sat} = 8{,}43\cdot10^4$ m/s, f = 2.5 GHz, P_D = 15 mW, Vdd = 1.8 V, R_{sheet} = 10 Ω/square, Wf= 2.5 μm, Q_{ind} = 10, $L_{g,bw}$= 1 nH, $Q_{ind,bw}$ = 50 and Leff = 0.16 μm (0.18 μm process).

From these expressions it's possible to plot the LNA's noise figure and gain curves overlaid (figure 3), which allows the search of best noise figure/gain pair from a given power consumption, frequency and gate inductor´s quality factor.

3. FEASIBILITY

Once the noise figure and transconductance are chosen for specified power consumption, frequency, gate inductor's quality factor and technology, all component values can be calculated. The problem is that changing any one of these parameters has impacts on LNA performance, to the point of rendering the methodology unreliable or unfeasible. Decreasing power consumption results in transistor being biased on weak inversion, where the whole set of equations used is no longer valid, and decreasing frequency makes the inductors too big for integration with the specified quality factor. So, it is necessary to investigate the impact of working with a lower inductor's quality factor (to ascertain that it can be integrated), lower frequency (for using other available bands), older technology (for lower price) and less power. The derived equations are used, yielding the results on Table I.

Table I shows that decreasing the operating frequency to 915 MHz impacts in the size of the gate inductor, which becomes more difficult to integrate. A reduced power consumption or an increased transistor channel length (technology downgrade) leads to a much smaller gain and a worse inductor quality factor, for integrated inductors, leads to a worse gain and inductor size. All this parameters together results in an LNA with lower gain, higher NF and with an inductor difficult to integrate. The overall result is not feasible. An all integrated LNA must have, at least, power consumption higher than 5 mW.

TABLE I. Impact of changing parameters on the LNA gain and noise figure.

Parameter	Original	Decreasing frequency	Decreasing power	Decreasing quality factor	Increasing channel length	All Together
f (GHz)	2.5	0.915	2.5	2.5	2.5	0.915
PD (mw)	15	15	5	15	15	5
Qind (Lg)	10	10	10	4	10	4
Lmin (µm)	0.18	0.18	0.18	0.18	0.35	0.35
Lg (nH)	4.25	12.8	3.1	15.1	3.1	9.21
W (mm)	1.885	1.855	1.7	3.9	1.15	2.87
NF (dB)	0.76	0.76	0.87	0.882	0.936	1.53
AV (dB)	14.88	15.46	8.46	11.16	8.56	8.68

4. RESULTS

Two different circuits were designed, one with off-chip inductors (LNA1) and other fully integrated (LNA2). Without integrated inductors the method tends to generate a large transistor which ends in weak inversion operation. This problem is attacked by adding the curve of transistor length to the noise figure and transconductance curves. In this way it is possible to keep transistors on strong inversion by making them no larger than certain value, as shown in figure 4 as vertical numbered lines. Choosing 0.276 V and 0,28 pF for v_{od} and C_{ex}, respectively, leads to a 199 µm transistors width, which guarantees operation on strong inversion and can results in a noise figure below 1 dB and transconducatance around 0,09 A/V (13 dB of power gain) for a 4 mW power consumption amplifier, as can be seen in figure 4. Nevertheless the gate inductor produced for this particular combination is around 65nH, which can't be integrated with a quality factor of 100.

For the fully integrated LNA, the inductor size is the worst constraint. Fortunately it can be observed by adding the gate inductor's size curve over the noise figure and transconductance plot, regardless the transistor width, as shown on figure 5.

In order to achieve the fully integrated LNA the power consumption was increased to keep transistors in strong inversion and increase the overall gain of the amplifier, with that it was possible to track the maximum allowable inductor's size for a fixed quality factor. Using 15 mW of power consumption on equation (3) and (4) produced the curves seen in figure 5.

Picking up v_{od} of 0.1 V, a C_{ex} of 0.1 pF leads to a integratable L_g of 9.8 nH, to 2.15 dB of noise figure and to 0.097 A/V of transconductance (13.7 dB power gain).

The simulation results were obtained using the RF BSIM3 model from 0.35 µm AMS (*AustriaMicroSystem*) process.

Comparing these results, it is possible to see the trade-off between power, noise figure and gain for chosing the partially or fully integrated low noise amplifier. If low power is the main requirement, adding an off-chip gate inductor is a good choice, but if cost is the primary goal, the fully integrated version should be considered depending on inductor's feasibility.

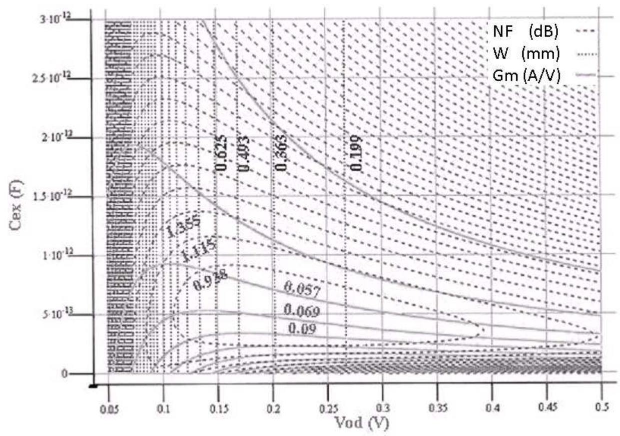

Figure 4. Overlaid plots of noise figure, tranconductance (gain) and transistor's length for constante power consumption. Parameter used were: $\gamma = 2$, $\delta = 4$, $c = j0.395$, $E_{sat} = 4.7 \cdot 10^6$ V/m, $v_{sat} = 8{,}43 \cdot 10^4$ m/s, f = 0.915 GHz, P_D = 4 mW, Vdd = 1.8 V, R_{sheet} = 8 Ω/square, Wf= 10 µm, Q_{ind} = 100, $L_{g,bw}$= 0 nH, $Q_{ind,bw}$ = 0 and Leff = 0.29 µm (0.35 µm process).

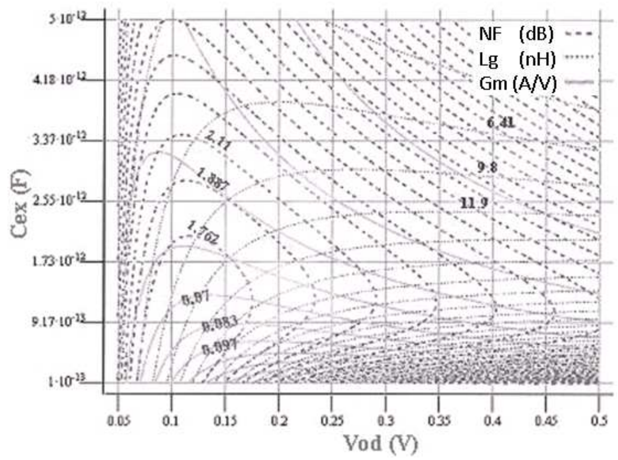

Figure 5. Overlaid plots of noise figure, tranconductance (gain) and inductor's size for constante power consumption. Parameter used were: $\gamma = 2$, $\delta = 4$, $c = j0.395$, $E_{sat} = 4.7 \cdot 10^6$ V/m, $v_{sat} = 8{,}43 \cdot 10^4$ m/s, f = 0.915 GHz, P_D = 15 mW, Vdd = 1.8 V, R_{sheet} = 8 Ω/square, Wf= 10 µm, Q_{ind} = 4, $L_{g,bw}$= 0 nH, $Q_{ind,bw}$ = 0 and Leff = 0.29 µm (0.35 µm process).

TABLE II. LNA1 and LNA2 results compared with other works

Ref	Technology (µm)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Frequency (GHz)	Integrated	Year
1	0,25	12	1.35	-4	2	0,9	Partially	2004
4	0,35	17	3,4	-5,1	13	0,9	Partially	2005
5	0,18	11,9	2,41	0,7	0,95	0,9	Partially	2006
6	0,18	14	2,3	-14	7,5	0,9	Fully	2007
7	0,35	18	4.6	4.6	32,4	0,945	Fully	2007
LNA1	0,35	10.11	1.37	-8,27	2,67	0,915	Partially	2010
LNA2	0,35	11.37	2.97	3.67	12,67	0,915	Fully	2010

5. CONCLUSIONS

In this work two different design optimization techniques were presented to find the best noise figure/gain pair for a given power consumption level, of fully and partially integrated LNA operating at 915 MHz. Using these techniques it was possible to design circuits with features comparable to other recent works. Also, it could be concluded that it's still not very advantageous to use on-chip integrated inductors for frequencies around 900 MHz, once the necessary inductors size typically has poor quality factor.

10. REFERENCES

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