DIGITAL PHASE LOCKED LOOP PROJECT FOR RADIO RECEPTOR APPLICATION

Tallita C. Sobral, João Paulo C. Cajueiro

Laboratório de Dispositivos e Nanoestruturas, Departamento de Eletrônica e Sistemas, Universidade Federal de Pernambuco. Rua Acadêmico Hélio Ramos, s/n, Várzea, 50740-530, Recife, PE, Brasil. Email: joaopaulo@ee.ufpe.br

ABSTRACT

This paper describes the development of a DPLL - Digital Phase Locked Loop, with the main blocks: PFD - Phase and Frequency Detector, Loop Filter, VCO - Voltage Controlled Oscillator and a 4-bit Frequency Divider. The system was fully developed on the free Electric software. Each block was simulated from schematic and from layout extracted netlist, including extracted parasitic elements. The complete integrated system was also validated by simulation with parasitic extraction. The results of simulations are analyzed for the layout and schematic showing good performance for application in a FM demodulator.

1. INTRODUCTION

A PLL, or Phase Locked Loop, is a widely used circuit in communication systems. In these systems, an internal clock is synchronized with an external signal (data signal or a clock) by use of a PLL. Other use is in clock recovery process, when a known frequency signal is received, you need a clock synchronized to the circuit that will process the input signal (the PLL locks in the in put frequency, generating the internal clock). Another very common application is the synthesis of frequency. In this application the PLL is used to generate a clock based on another. Usually the generated clock has a frequency multiple signal taken as reference. In this work the PLL is used for FM demodulation, where the change in frequency is obtained from the VCO output when the PLL is locked.

A DPLL (Digital Phase Locked Loop) differs from the PLL simply because its use to synchronize digital signals. A DPLL is a system where the phase comparator is composed of digital components. Furthermore, a DPLL differs form an analog one by the delay introduced by the frequency divider and the nonlinear effects introduced by the phase comparator.

This paper develops a DPLL for application in FM radio receiver, running at a frequency of 4.5 MHz, considering the supply voltage of 3.3V and a 4 bits frequency divider. The technology utilized was 0.35µm.

2. DPLL BLOCKS

The DPLL is basically composed of four blocks: Phase and Frequency Detector (PFD), Filter, Voltage Controlled Oscillator (VCO) and Frequency Divider. The diagram in Figure 1 represents the DPLL system with his blocks and interconnections between them.

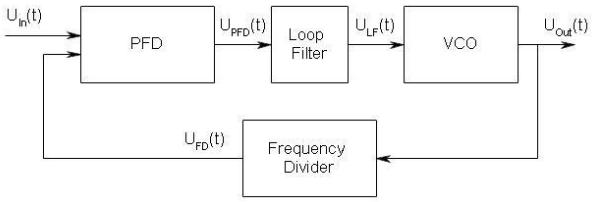

Figure 1 DPLL Block Diagram

2.1. Phase and Frequency Detector

The Phase and Frequency Detector or PFD consists of two D latches working at rising edge, a two-input NAND gate and two MOSFETs, one NMOS and other PMOS, to drive the VCO (as in Figure 2). The D latches input are always connected to VDD and the input clocks are the DPLL input signal, *data*, and the output signal of the frequency divider, *dclock*, that we want synchronize with the input. The latch that receives *data* output is called *Up*, while the output of the latch that receives *dclock* is called *Down*. The diagram of Figure 2 shows when the input signal *data* is ahead of *dclock*, the signal *Up* stay high until the next rising edge in *dclock*. Likewise, if *dclock* is ahead, *Down* remains high until the occurrence of the next rise in the *data* signal.

The *Up* and *Down* signals are inputs of a NAND gate, generating a clear signal to the laches, so that the next rising edge of *data* or *dclock* can clear the latches.

The signals *Up* (inverted) and *Down* feed the gates of PMOS and NMOS transistors respectively. So when the *data* signal is earlier, the output voltage is loaded toward VDD because the PMOS is open and NMOS closed. The increased voltage across the capacitor, which represents the control of the VCO, will increase the frequency of the oscillator. Similarly, when *dclock* is advanced, NMOS is open and PMOS closed, causing the voltage on the capacitor decrease, decreasing the control voltage, thereby reducing the frequency of the VCO.

2.2. Filter

The filter is a simple first order RC low-pass. With a 30kΩ resistor and a 100pF capacitor, the filter has a 3dB frequency at 53kHz.

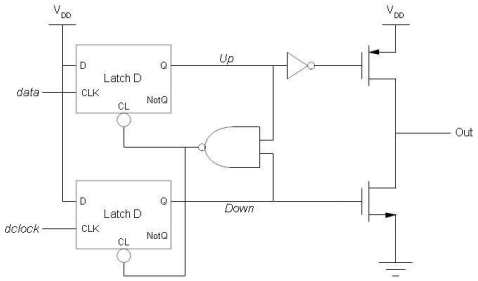

Figure 2 PFD Block Diagram

2.3. Voltage controlled Oscillator

This oscillator is similar to a ring oscillator, but with the frequency of oscillation controlled by current through the inverter (current starved inverter, as shown in Figure 3). The proposed oscillator is implemented by 3 such inverters and three capacitors to reduce the frequency of oscillation, as show in Figure 4.

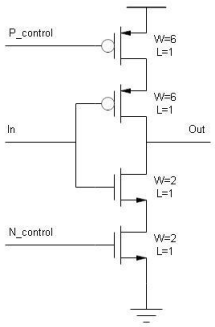

Figure 3 Current Starved Inverter Diagram

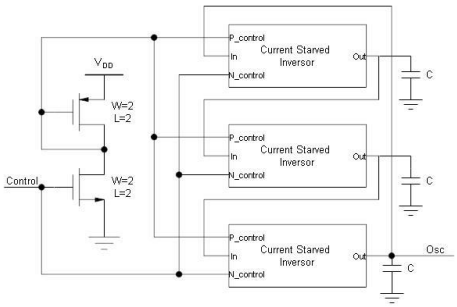

Figure 4 Voltage Controlled Oscillator Diagram

For our application, the VCO output is the desired output signal, so a six inverters buffer (not shown) is used to give ability to transmit power to the load.

2.4. Frequency Divider

The frequency divider circuit divides the frequency of the VCO output to feed the input of the PFD, this signal, called *dclock*, will synchronize with the input signal *data*. This frequency divider has four input bits that can be programmed so as to divide the input frequency 1 to 16 times. The frequency divider consists of three basic parts, a 4-bit synchronous counter, an array of XNOR gates that are activated with the input bits, and a 4 input NAND gate.

The NAND gate output is connected to a D flip-flop activated on falling edge of the clock. The flip-flop output clears the counter. Since the counter operates at the rising clock, the frequency divider keeps the output in high level during half period of the input signal. That is, every N periods of the input clock, the output is 1/2 clock period in high level and (N-1/2) clock periods in low level, where N is the counter programmed number $[N_0N_1N_2N_3]$.

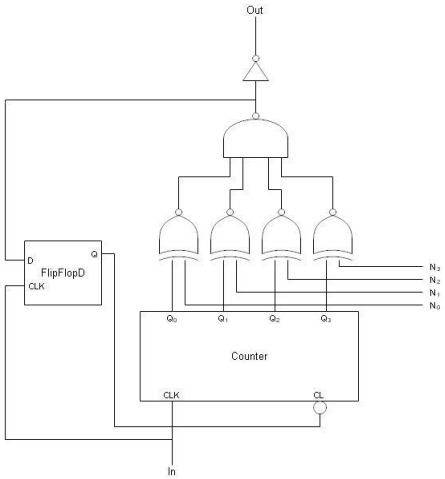

Figure 5 Frequency Divider Diagram

3. DPLL LAYOUT

The DPLL system was designed using the software Electric VLSI Design System, version 8.07. Figure 6 shows the PFD layout. The low-pass filter was built with the NWELL resistor, where the resistance is 1kΩ/square, and a CPOLY capacitor (POLY1-POLY2).

Voltage Controlled Oscillator was build from three Current Starved Inverter blocks, three capacitors (400fF) and two MOSFETs to control the current polarization of the oscillator. Figure 7 shows the VCO layout.

The frequency divider was constructed with a 4 bits counter, 4 XNOR gates, a 4 input NAND and a D Flipflop. Figure 8 shows the 4 bits Frequency Divider layout. Figure 9 shows the layout of the DPLL system with all the blocks PFD, Filter, VCO, Buffer and Frequency Divider.

4. SIMULATION AND RESULTS

The simulations were done in the DPLL and some blocks. Blocks that were separately simulated were the Voltage Controlled Oscillator with the output Buffer (Buffer & VCO) and the 4 bits Frequency Divider (FreqDivider4). The extraction of the parasites was done considering only area and perimeter devices information. The simulator SpiceOpus Light version 2.25 was used to

perform the functional verification of the blocks and the entire system.

4.1. VCO & Buffer Simulation

The Figure 10 shows the simulation result of VCO & Buffer. In this simulation, a signal was applied in VCO input control pin from 0V to 3.3V, with 0.33V step. The Table 1 shows the output VCO frequency with respective control input voltage, for schematic and layout simulation.

$V_{Control}$ [V]	f_{VCO} (Sch) [MHz]	f_{VCO} (Lay) [MHz]
0.99	9.09	9.01
1.32	18.11	18.28
1.65	26.52	26.67
1.98	31.54	31.75
2.31	33.90	34.25
2.64	35.21	35.59
2.97	36.10	36.49
3.30	36.90	37.17

Table 1 VCO Input Voltage Control and Output Frequency – Schematic and Layout

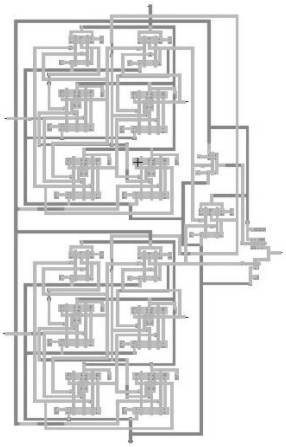

Figure 6 PFD Layout

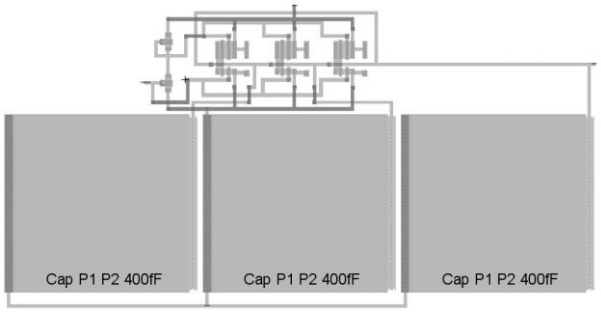

Figure 7 VCO Layout

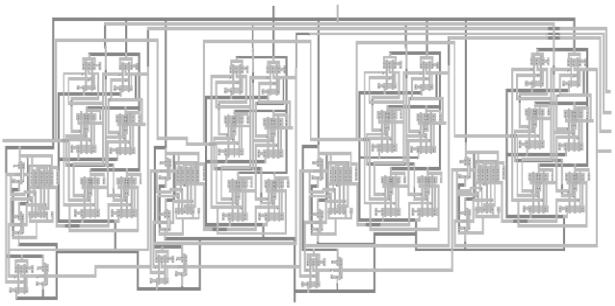

Figure 8 Frequency Divider Layout

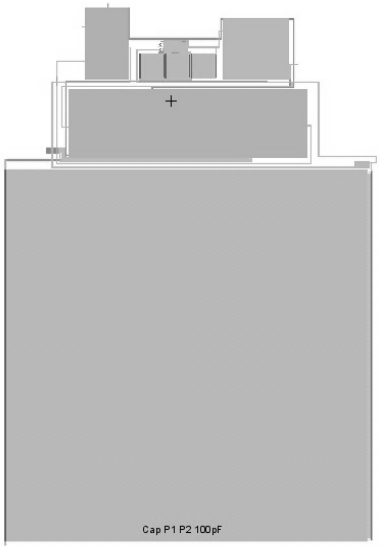

Figure 9 DPLL Layout

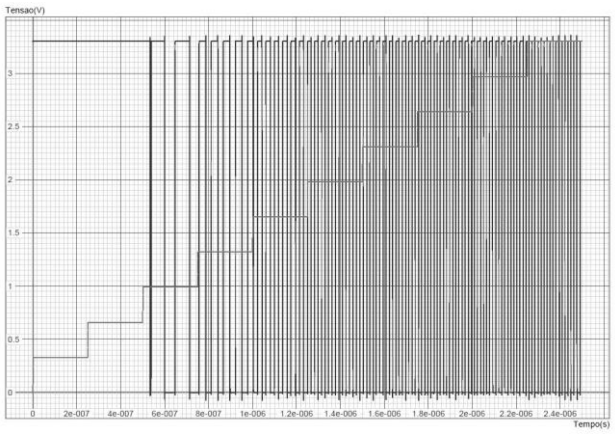

Figure 10 VCO & Buffer Simulation

4.2. Frequency Divider Simulation

The frequency range of the VCO output signal is between 9MHz and 37MHz, as shown through simulations in the above item (Table 1). For the DPLL to work in 4.5 MHz, the division factor used in the frequency divider is 4. This way, the output frequency range of frequency divider is from 2.25 MHz to 9.25 MHz. The factor N applied in frequency divider is 3, because the output of the divider operates with a one input pulse at high level and N input pulses at low level.

4.3. DPLL Simulation

The Figure 11 shows the DPLL input signal, with 0.22µs period, and the output signal of low-pass filter. The system synchronizes the frequency divider output (*dclock*) with the DPLL input signal (*data*). When *data* and *dclock* signals are synchronized, the filter output maintains a constant voltage. The Table 2 shows the value of this voltage for an input frequency between 2.5 MHz and 9MHz.

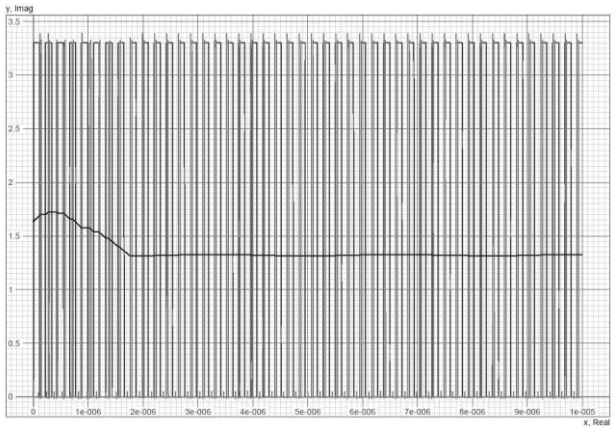

Figure 11 DPLL Schematic Simulation

5. ANALYSIS

The DPLL schematic and layout were simulated for various input frequencies, so that could be evaluated PDLL system behavior within a frequency band of input and compared the behavior of the system in schematic and layout. Table 2 contains the average value (DC) output voltage of the low-pass filter for the DPLL schematic and layout, within a frequency range of the input signal of 2.5 MHz to 9MHz.

Table 2 shows an average error between filter output voltages for schematic and layout system about 0.012 V. The low-pass filter output voltage is applied directly to the VCO control input, controlling its output frequency. Through VCO simulations was observed that its output frequency varies from 37 MHz to 9 MHz, approximately, for control voltage ranging from 0.99 V to 3.3 V. As we are considering, the factor of division for Frequency Divider is four (N = 3). The frequency range of output signal frequency divider is from 2.25 MHz to 9.25 MHz. This gives a DPLL operation band of 7 MHz.

f_{in} [MHz]	**$Vout_{Sch}$** [V]	**$Vout_{Lay}$** [V]	**Error** ($Vout_{Lay-Sch}$) [V]
9	2,907	2,963	0,056
8,5	2,383	2,342	0,041
8	2,046	2,053	0,007
7,5	1,867	1,874	0,007
7	1,760	1,743	0,017
6,5	1,639	1,649	0,010
6	1,547	1,552	0,005
5,5	1,467	1,469	0,002
5	1,389	1,396	0,007
4,5	1,326	1,326	0,000
4	1,245	1,247	0,002
3,5	1,175	1,174	0,001
3	1,108	1,110	0,002
2,5	1,022	1,037	0,015

Table 2 DPLL Output for Input Frequency range - Layout and Schematic

The area occupied by the DPLL circuit and the portion of each main block are detailed in Table 3.

Area [μm^2]	**Block**	**A_{block}/A_{DPLL}** [%]
2640,90	PFD	1,5
123264,03	Filtro	70,02
2733,10	VCO	1,55
3409,37	Buffer	1,93
14161,38	FreqDivider	8,04
176038,75	DPLL	100

Table 3 DPLL Area and Blocks Area

6. CONCLUSION

This paper presented a DPLL configuration focusing applications in radio receivers. The schematic of the system was simulated and the layout designed and validated for a range of input frequency of 2.5 MHz to 9 MHz. Within this range, the system was functioning consistent with expectations, generating an output voltage between 1V and 3V.

7. REFERENCES

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[3] Ulrich L. Rohde, *Digital PLL Frequency Synthesizers – Theory and Design*, Prentice-Hall, 1983.