A TRIANGULAR WAVEFORM GENERATOR USING THE TRANSLINER LOOP PRINCIPLE

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ABSTRACT

This work proposes the implementation of a low voltage, low power, triangular current wave generator based on the translinear loop topology with the MOSFETs operating in weak inversion. The generator is intended to be used in a pulse width modulation block of a class D amplifier for hearing aid devices. The circuit was designed in the AMS 0.35 µm CMOS technology. The correct operation of the system was verified through simulations in the Mentor Graphics CAD tools. A minimum power supply voltage of 1.1 V was achieved with a power consumption of 15.4 µW. The active area of the triangular wave generator is 0.024 mm^2.

1. INTRODUCTION

The translinear loop principle (TLP) was described by Barrie Gilbert in 1975 [1]. This principle analyzes the (steady-state) large-signal characteristics of translinear loops usually with a few lines of algebra, considering only the currents flowing throw the translinear elements. A translinear element (TE) is characterized by an exponential relationship between the current and its control voltage

$$I_k = \lambda_k \, e^{\beta V_k} \tag{1}$$

At the beginning this principle was used in BJT transistor circuits, but it has been applied to MOS transistors operating in weak inversion due to the exponential relationship between current and voltage. Consider the closed loop of N ideal TEs, shown in Fig. 1, we classify a clockwise element when the control voltage drop is in the arrow direction and a counterclockwise element when is in the opposite direction. Let us denote by *CW* the set of clockwise-element indices and by *CCW* the set of counterclockwise-element indices. Applying the voltage Kirchoff law to the loop gives

$$\sum_{i \in CW} V_i = \sum_{j \in CCW} V_j \tag{2}$$

Substituting (1) into (2), the common factor β is cancelled and applying the logarithmic sum-product property we obtain a product current equation.

$$\prod_{i \in CW} \left(\frac{I}{\lambda} \right)_i = \prod_{j \in CCW} \left(\frac{I}{\lambda} \right)_j \tag{3}$$

The translinear principle states that the product of the currents flowing through the *CW* elements is equal to the product of the currents flowing through the *CCW* elements [2].

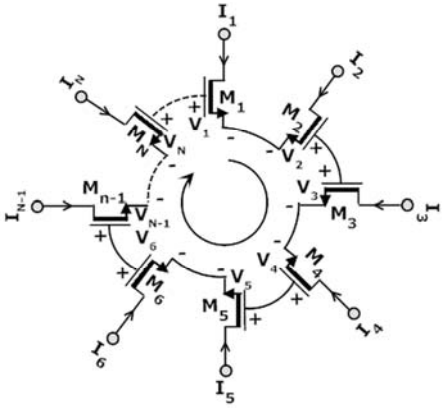

Fig. 1. Translinear loop with N transistors.

2. THE MOSFET MODEL

The MOSFET compact model used here, which describes the behavior of the device in all its operating regions, is based on the inversion charge density [3]. According to this model, the drain current of a long channel transistor can be split into the symmetric forward (I_F) and reverse (I_R) components, which are dependent on the voltages applied to the terminals, technological parameters (*TP*) and the aspect ratio (*S*) as given below

$$I_D = I_F \left(V_{GB}, V_{SB}, S, TP \right) - I_R \left(V_{GB}, V_{DS}, S, TP \right) \tag{4}$$

The forward and reverse currents can be described in terms of the forward (i_f) and reverse (i_r) inversion levels, according to.

$$I_{F(R)} = I_{SH} \, S \, i_{f(r)} \tag{5}$$

$$I_{SH} = \mu_n C'_{ox} n \frac{\phi_t^2}{2} \tag{6}$$

$$S = \frac{W}{L} \tag{7}$$

The relationship between the inversion levels and the voltages is called the UICM equation (8), where V_P is the pinch-off voltage, and V_{T0} the zero bias threshold voltage.

$$V_P - V_{S(D)} = \phi_t \left[\sqrt{1 + i_{f(r)}} - 2 + \ln \left(\sqrt{1 + i_{f(r)}} - 1 \right) \right] \tag{8}$$

$$V_P \cong \frac{V_{GB} - V_{T0}}{n} \tag{9}$$

When the transistor operates in saturation, the reverse current is negligible with respect to the forward current and the drain current is almost independent of the drain voltage, *i.e.*

$$I_D \cong I_{F(R)} = I_{SH}\, S\, i_f \tag{10}$$

When the transistor operates in weak inversion (i_f< 0.1), the drain current can be expressed as

$$I_D = I_0\, e^{\left(\frac{V_G - V_S n}{n\phi_t}\right)} e^{-\frac{V_{T0}}{n\phi_t}} \tag{11}$$

$$I_0 = 2\, I_{SHN} S\, e^{1} \tag{12}$$

The saturation voltage $V_{DS\,sat}$ is approximated by

$$V_{DSsat} = \phi_t \left(\sqrt{1 + i_f} + 3\right) \tag{13}$$

More details regarding (4)-(13) can be found in [4].

3. DESIGN EQUATIONS

In order to explain the operating principle of the TL, consider the four transistors shown in Fig. 2.

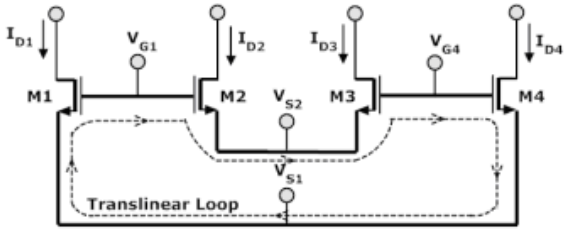

Fig. 2. Translinear loop with four transistors.

Applying (2) to this example we get

$$\left(V_{G1} - V_{S1}\right) + \left(V_{G3} - V_{S3}\right) = \left(V_{G2} - V_{S2}\right) + \left(V_{G4} - V_{S4}\right) \tag{14}$$

Assuming that all the transistors of the TL operate in weak inversion ($i_f \leq 0.1$) and saturation, the gate voltage can be written as

$$V_G = V_{T0} + V_S n + n\phi_t \ln\left(\frac{I_D}{I_0}\right) \tag{15}$$

Since V_{S1}=V_{S4}, V_{S2}=V_{S3} and all the transistors have the same threshold voltage, the substitution of (15) to (14) leads to

$$\begin{aligned} &n_1 \ln\left(\frac{I_{D1}}{I_{01}}\right) + V_{S1}\left(n_1 - 1\right) + n_3 \ln\left(\frac{I_{D3}}{I_{03}}\right) + V_{S2}\left(n_3 - 1\right) = \\ &n_2 \ln\left(\frac{I_{D2}}{I_{02}}\right) + V_{S2}\left(n_2 - 1\right) + n_4 \ln\left(\frac{I_{D4}}{I_{04}}\right) + V_{S1}\left(n_4 - 1\right) \end{aligned} \tag{16}$$

If the TL gate voltages are designed to be close to each other ($V_{G1} \approx V_{G4}$), the slope factors n_1=$n_2 \cong n_3$=n_4 [1]. Then, expression (16) is reduced to:

[1] n is slightly dependent of the gate voltage [3]

$$\left(\frac{I_{D1}}{I_{01}}\right)\left(\frac{I_{D3}}{I_{03}}\right) = \left(\frac{I_{D2}}{I_{02}}\right)\left(\frac{I_{D4}}{I_{04}}\right) \tag{17}$$

Finally, after canceling out the common terms in I_0, a multiplicative relationship among the inversion levels of the transistors taking part in the TL is obtained:

$$i_{f1}\, i_{f3} = i_{f2}\, i_{f4} \tag{18}$$

4. TRIANGULAR CURRENT WAVE GENERATOR

A triangular current wave generator was designed based on the TL principle [5]. In Fig. 3, we represent the block diagram of the circuit, basically the integration of a fixed current (I_{ref}) which changes its sign when it either reaches a maximum ($I_{tri\ max}$) or a minimum ($I_{tri\ min}$)

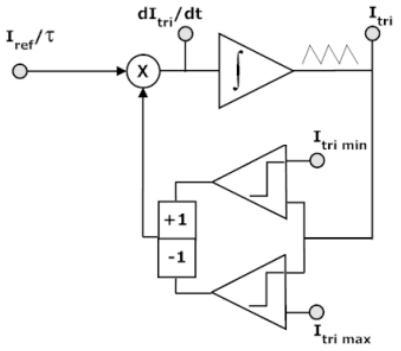

Fig. 3. Block diagram of the triangular current wave generator.

Analyzing the block diagram, we obtain the equations (19) and (20).

$$\frac{dI_{tri}}{dt} = \pm\frac{I_{ref}}{\tau} \tag{19}$$

$$T_{tri} = 2\tau\frac{\left(I_{tri\max} - I_{tri\min}\right)}{I_{ref}} \tag{20}$$

If the triangular current I_{tri} flows through a translinear element (1), its derivate can be expressed as

$$\frac{dI_{tri}}{dt} = \beta I_{tri}\frac{dv_{tri}}{dt} = \pm\frac{I_{ref}}{\tau} \tag{21}$$

where, in the weakly inverted MOSFET, β=1/$n\phi_t$. Considering the triangular voltage (v_{tri}) as being synthesized as a capacitor voltage leads (21) to

$$I_{tri}\frac{dv_{tri}}{dt}C_{tri} = \frac{I_{ref}}{\tau\,\beta}C_{tri} \rightarrow I_{tri}\, I_C = I_{ref}\, I_{tun} \tag{22}$$

where

$$I_C = C_{tri}\frac{dv_{tri}}{dt}; \quad I_{tun} = \frac{C_{tri}}{\tau\,\beta}$$

4.1. Design methodology

Expression (22) can be implemented with the translinear loop circuit in Fig. 4, being M_1, M_2, M_3 and M_4 the TEs.

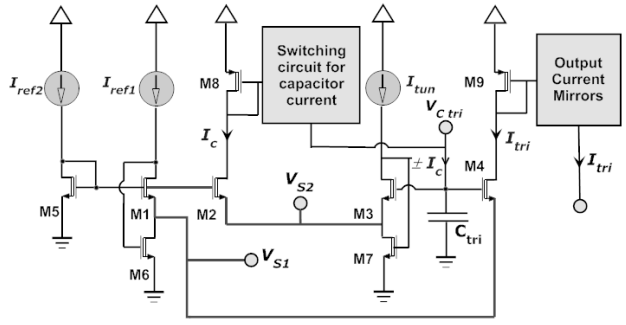

Fig. 4. Translinear loop of the triangular current wave generator.

For this circuit the I_{tun} current is

$$I_{tun} = \frac{C_{tri} n \phi_t S_{mt}}{\tau} \qquad S_{mt} = \frac{S_1 S_3}{S_2 S_4} \tag{23}$$

The design reference currents are: $I_{ref1} = I_{ref2} = I_{tun} =$ 1 μA and the average value of $I_{tri} = 6$ μA with a peak to peak value of 8 μA. The inversion level of M_1 is 0.1. Thus, applying (5) results in $S_1 = 120$[2].

$$I_{D1} = 1\,\mu\text{A} \text{ and } i_{f1} = 0.1 \rightarrow S_1 = 120$$

To achieve a minimum supply voltage of 1.1 V, the saturation voltage of M_6 should be low; for this design, we have chosen V_{DSsat6}<125 mV, which means i_{f6}<3 (13). To guarantee the saturation of M_6, the value of V_{S1} is designed with a safety margin of 50 mV (α = 2, V_{S1} = 175 mV). Now, solving (24) we can find i_{f5} [6].

$$\sqrt{1+i_{f5}} - 1 = \left[\sqrt{1+i_{f6}} + 3 + \alpha\right] + \left[\ln\left(\frac{\sqrt{1+i_{f1}} - 1}{\sqrt{1+i_{f5}} - 1}\right)\right] \tag{24}$$

The calculated inversion level is i_{f5} = 14.6 for i_{f6} = 1.29, corresponding to aspect ratios of $S_5 = 0.8$ and $S_6 =$ 120.For M_7 we have chosen the same aspect ratio of M_6, which leads to a lower saturation voltage due to its lower current (V_{DSsat7}= 102 mV, i_{f7}=0.235). Because voltages V_{G1} and V_{G4} should be about the same (to neglect differences among the slope factors), the inversion level of M_4 is designed equal to that of M_1 for the average triangular current (6 μA). The resulting aspect ratio is S_4 = 720.

$$\overline{I}_{D4} \simeq 6\,\mu\text{A} \text{ e } i_{f4} = 0{,}1 \rightarrow S_4 = 720$$

Because the value of V_{S2} varies with I_{tri} we must guarantee the saturation of M_7 for the lower triangular current ($I_{tri\,min}$=2 μA). To achieve this, we have designed the inversion level of M_3 slightly smaller than that of M_4, obtaining S_3 = 300, equivalent to an inversion level of 0.04. This difference leads to

$$V_{S1} - V_{S2} = \phi_t \quad (\phi_t = \text{thermal voltage})$$

Finally, the aspect ratio of M_2 is obtained by the parameter S_{mt} which is adjusted to get a frequency of 200 kHz. The aspect ratio after adjusting is S_2 = 90.

[2] V_{T0N} = 560mV, I_{SQN} = 85nA e n_n = 1.25 (AMS 0.35 μm)

4.2. Minimum supply voltage

The supply voltage is restricted by the inequalities (25) and (26).

$$V_{dd} > |V_{GS9}| + V_{DSsat4} + V_{S1} \tag{25}$$

$$V_{dd} > |V_{GS8}| + V_{DSsat2} + V_{S2} \tag{26}$$

The saturation voltage plus the source voltage was designed to not exceed 0.3 V; thus, to operate from 1.1 V supply voltages the values of $|V_{GS8}|$ and $|V_{GS9}|$ have to be both lower than 0.8 V. Applying (8) to M_8 and M_9 we obtain the maximum inversion levels for these transistors.

$$i_{f8}\,,\, i_{f9} \le 8$$

Transistor M_9 conducts the triangular current (2μA-10μA), while M_8 conducts I_C, which is lower than I_{tri}. Thus, the critical transistor is M_9 with an aspect ratio bigger than 41.6[3].

$$i_{f9} \le 8 \quad S_9 = \frac{I_{D9\max}}{i_{f9}\, I_{SQP}} \rightarrow \quad S_9 \ge 41.6$$

The switching circuit for the capacitor current and the Schmitt-trigger circuit for controlling the minimum and maximum triangular current are described in detail in

5. SIMULATIONS AND RESULTS

The circuit was designed in the AMS 0.35 μm technology. Transient simulations including Monte Carlo analysis were run in Mentor Graphics tools to validate the design. Fig. 5 shows the simulation of the triangular current, the nominal frequency of 200 kHz, was adjusted by parameter S_{mt}. The need for this tuning is due to four effects: difference between the maximum/minimum real current triangular values and the theoretical (caused by the delay in the current comparison) value, parasitic capacitance of the node, multiplication errors in the translinear loop and the switching time of the charging current of the capacitor.

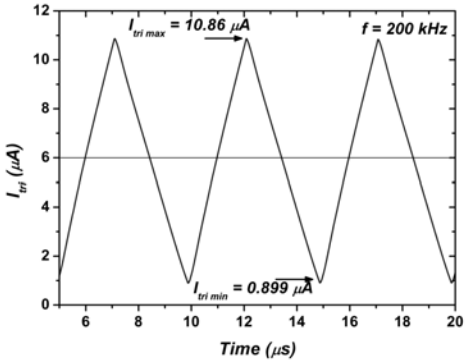

Fig. 5. Simulation of the triangular current.

Fig. 6 illustrates the current and voltage on the capacitor, showing that a variation of the triangular current of 9.961 μA corresponds to a voltage swing of only 93 mV.

[3] V_{T0P} = -740mV I_{SQP} = 30nA e n_p = 1.3 (AMS 0.35 μm)

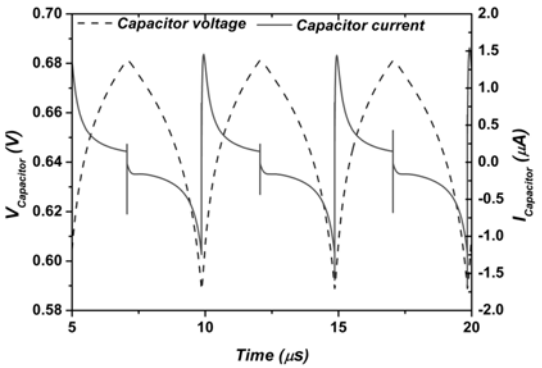

Fig. 6. Simulation of the current and voltage on the capacitor.

Fig. 7 summarizes the Monte Carlo simulation of the periodic triangular wave, with an average value of frequency of 200 kHz and a standard deviation of 7 kHz. This represents a relative error less than 7% for 95% of the cases (± σ).

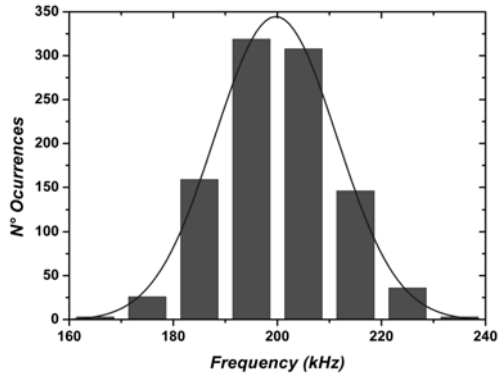

Fig. 7. Monte Carlo Simulation of the frequency at V_{dd} = 1.4V (1000 samples).

Finally, the simulation for the worst speed case shows the lowest operating frequency at 167 kHz and the worst power case the highest frequency at 266 kHz. The minimum power consumption is 15.4 μW at a power supply of 1.1 V.

6. LAYOUT

Layout techniques were used during the design to minimize parasitic resistance and capacitance, like employing folded transistors, controlling the metal path width and avoiding the crossing between different metal layers [7].

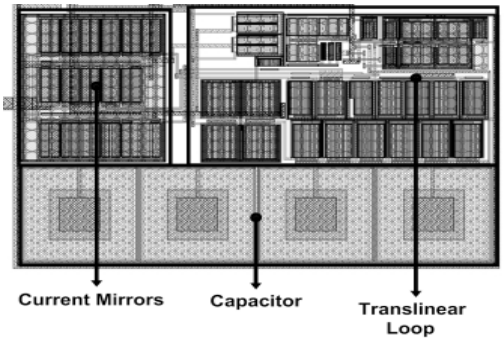

Fig. 8. Layout of the triangular wave generator.

To reduce mismatch effects common-centroid geometries, interdigitated and series association of transistors were applied. To decrease the voltage threshold (V_{T0}) dependence on the transistor's dimensions, only two channel lengths (1μm and 4 μm) and three channel widths (4 μm, 10 μm e 20 μm) were used for analog blocks. The final layout of amplifier (blocks and routing) is shown in Fig. 8 with a total area of 0.024 mm^2.

7. CONCLUSIONS

A low voltage, low power triangular current generator was designed exploring the translinear loop principle with the MOSFET model equations. Using a compact model allows a project that take into account the trade-off of among area, power consumption and maximum operation frequency of the generator. The design equations are process independent and reproducible in any standard CMOS technology. Simulations show low power consumption and correct operation at supply voltages down to 1.1 V in 0.35 μm technology. The nominal frequency is 200 kHz, but its value is dependent on technological variations, reaching a minimum value of 167 kHz for the worst speed case and 266 kHz for the worst power case. However, this variation is not detrimental to its application in a class-D amplifier.

8. ACKNOWLEGMENT

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