GATE OXIDE LEAKAGE AND SUBTHRESHOLD CURRENT ANALYSIS IN DIFFERENT CMOS TECHNOLOGIES

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ABSTRACT

In this work is presented a methodology to analyze the leakage current in CMOS technology. Process parameters, transistor sizing, transistor stacks are evaluated, as well as a set of significant logic gates. Different PTM processes have been considered to demonstrate and validate the proposed methodology.

1. INTRODUCTION

The advances in the integrated circuits (IC) industry are more and more scaling the CMOS technology. Smaller the transistor more transistor can be placed in the same area of silicon. Despite of all the improvements with this aggressive scaling, undesired nanometer effects have appeared. These effects normally interfere in the circuit performance and/or in the power consumption.

IC designers need CAD tools to support their decisions about the circuit design [6]. These tools help the designer to obtain important information like the time delay of gates, the critical paths in logic blocks, the power consumption, and so on. Furthermore, the designer needs to chose which technology fits better in the circuit requirements. In order to do that, he has to analyze all the constraints, like dynamic and static power dissipation, as well as the delay time of logic gates [1]. This paper focuses on the static consumption evaluation, more precisely in the leakage currents.

This paper has the main objective of introducing a methodology to analyze the leakage current of CMOS processes, being a powerful tool to compare different technologies and support project decisions. In order to analyze the leakage currents in a specific technology it is not enough to simulate one circuit and verify how much static power it consumes. To do such evaluation the designer have to take into account some physical effects like DIBL, body effect and stack effect [1][11]. Moreover, he has to know if the scaling of transistor makes the subthreshold density current variate, or even evaluate the behavior of a set of logic gates in the addressed technology. This methodology is proposed to organize these simulations in a set of steps well defined in a way to help the designer to make decisions about which technology adopt in the project.

To a better understanding of the reader, Section 2 provides briefly the technical background of this work. The methodology of analysis is described in Section 3. In Section 4 some experimental results are shown in order to demonstrate the possibilities offered by the proposed environment. Conclusions and future works are outlined in Section 5.

2. BACKGROUND

Ideally CMOS gates present power consumption only when the gate output switches from a state to another. In real CMOS gates when they are not switching there are some static power dissipation due to subthreshold currents. However, it can be ignored in older technologies, larger than 130nm, due to the very low values [1].

Dynamic power consumption has two mechanisms: the charge of load capacitance and the short-circuit current when both PMOS and NMOS are partially conducting.

Static power consumption, in turn, has three major static currents components: tunneling gate oxide current, subthreshold current and reverse-biased junction current [7], These currents are illustrated in Fig. 1. There are also other leakage currents, but in normal operation mode they can be neglected [2]. In modern technologies even the reverse biased current can be neglected [7].

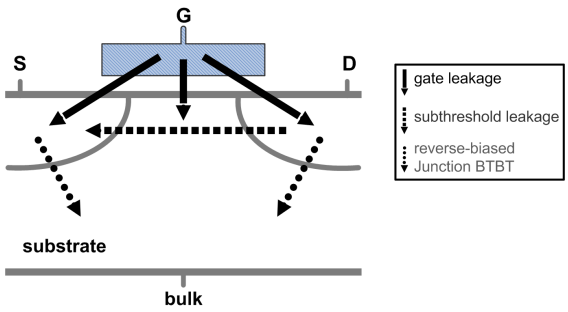

Figure 1: Leakage mechanisms in MOS transistor.

Subthreshold current happens when the gate bias is below to the threshold voltage. This current is dependent of process and geometry of transistor. The main effect that make this current change is the drain-induced barrier lowering (DIBL) and the body effect [8]. The first one makes the subthreshold current increase and the second makes it decrease (stack effect) [1][11].

The gate leakage, on the other hand, becomes an important factor for oxide thinner than about 15-20Å. Indeed, the gate leakage can become comparable to the subthreshold current. In Section 4 is shown that for some circuits, like 5-inputs NOR gate, it represents 98% of the total leakage current.

In order to perform a correct simulation of these parasitic currents, one has to know about the transistor model is being used. For instance, Model cards with MOS parameters for BSIM3 and BSIM4 are vety common, but only the BSIM4 one supports to calculation of tunneling gate currents [3][13]. The results presented in Section 4 were obtained by using predictive model cards [4] which uses BSIM4 model.

3. METHODOLOGY OF ANALYSIS

The methodology of analysis to the leakage current is versatile. It is used to evaluate the leakage current in processes using 4 different metrics. The first one is related to the extraction of parameters of a single transistor like subthreshold current density. The second step evaluates the relation between the leakage current and the scaling of the transistor channel width (W) in the each type of MOS transistor (PMOS and NMOS). The next step aims the evaluation of the stack effect and its influence in the total leakage current, analyzing separately gate oxide leakage and subthreshold current. Finally, in the last step is evaluated the leakage in a significant set of logic gates. Such information is enough, for example, to evaluate an estimative model [5][8], or to compare different processes, which is the focus of this paper. Each analysis step is discussed in more detail bellow.

Process analysis: Process characteristics are important for designer to know the viability of the process to specific project. This step gives to designer information about two important effects in the evaluation of leakage which are DIBL and body effect. Another parameters presented are the current densities of gate and subthreshold. With these ones are possible to figure out some characteristics of the transistors fabricated in the target technology.

Scaling analysis: In the previous step the densities were calculated, but the interest of this analysis is to know if the current really follows the scaling dictated by the density, or if it varies with the w variation, to such that in this analysis inverters are used. The currents are simulated to different drive strengths to high logic value and low logic value, in order to obtain data about both NMOS and PMOS transistors, respectively.

Stack analysis: The stack effect is an important effect to the subthrshold current behavior [1][7]. Although trasistor stacks decrease the performance of logic gate, the stack effect decreases the subthreshold current. It is indispensable to know what happens with the leakage current when the number of transistor in stacking increases. In order to perform such analysis, NAND and NOR gates have been considered, where the first one represents the stack in pull down plan and the second one represents the pull up plan. The stack has been increased up to five devices. This step gives three values: gate oxide leakage, subthreshold current and total static current.

SP and NSP analysis: The last step of the proposed methodology is a coverage analysis. It is important to know the behavior of a representative set of gates. The gates simulated in this step are the gates belonging to the ‘genlib-44_6’ list, considering the function with up to five variables[12]. It is a representative set because they represent all gates with up to five inputs, at most 4 stacked transistors and no literal repeated. The analysis also inclidues a set of nine gate built using non-series-parallel (NSP) networks [9].

All these four steps, described above, were automated through a set of shell scripts.

4. EXPERIMENTAL RESULTS

The proposed analysis was applied to three predictive technologies (PTM): 130 nm, 65 nm and 32 nm [4]. Due to the space limitation, the data presented in this work represents only some examples of output information provided by the environment; there are other information and graphics that can be extracted in each step.

The first results presented are about the parameters of technology.

In this step of analysis the focus are in five parameters: ‘n’ is the DIBL effect coefficient; ‘y’ is the body effect coefficient; ‘is0’ is the subthreshold current density; and ‘ig(on and off)0’ is the gate current density when the transistor is on or off, respectively. In Table 1 can be seen the behavior of this 5 parameters with the technology scaling. Each technology is simulated to a set of power supply values (Vdd) and temperatures. In Fig. 2 can be seen the variation of subthreshold of PMOS with the variation of temperature.

Table 1: Parameters extracted for technologies.

Parameters	PTM_130	PTM_65	PTM_32
W (μm)	0.160	0.120	0.030
L (μm)	0.120	0.060	0.090
Vdd (V)	1.200	1.000	0.900
np	0.150	0.230	0.263
nn	0.120	0.180	0.203
yp	0.190	0.170	0.161
yn	0.230	0.210	0.192
is0p (mA/m^2)	0.840	0.770	0.284
is0n (mA/m^2)	2.000	2.250	1.370
igon0p (mA/m^2)	4.000	4.580	5.950
igon0n (A/m^2)	6.920	3.690	2.780
igoff0p(mA/m^2)	0.850	2.170	2.960
igoff0n (A/m^2)	1.530	0.800	0.537

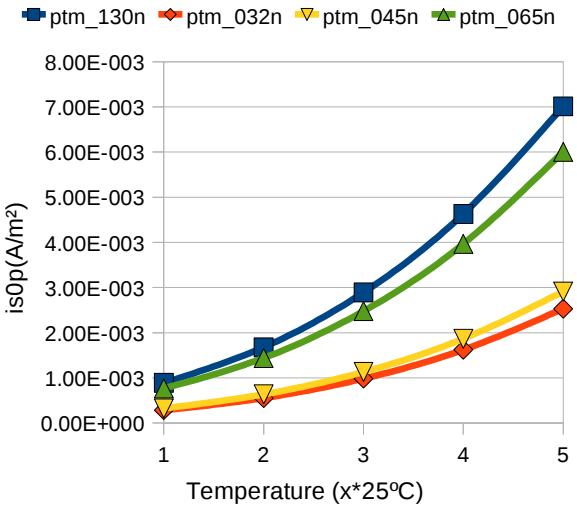

Figure 2: 'is0p' parameter X temperature variation.

In the second analysis the main focus is to examinate the relation between the leakage current and the scaling of width. In Table 3 can be seen that the relationship between the current and the scaling of W is almost 2x in all cases, for input = 0 (NMOS analysis). But is not constant when the technology is scaled.

Table 2: Current leakage X transistor scaling to input equal low logic value.

Drive Strength	PTM_130 (µA)	PTM_65 (µA)	PTM_32 (µA)
X1	0.016	0.0361	0.017
X2	0.033	0.0756	0.0361
X3	0.050	0.0115	0.0552
X4	0.067	0.0155	0.0743
X5	0.084	0.0194	0.0934
X6	0.101	0.233	0.113
X7	0.118	0.273	0.132
X8	0.135	0.312	0.151
X9	0.157	0.352	0.170
X10	0.169	0.391	0.189

The stack analysis could be seen the importance of gate leakage in the total leakage current. It is well know that because of the body effect in stacked transistors the subthreshold current goes down. Although with the decrease of subthreshold current the gate current takes place in the total current. Table 3, and Table 6 (for NAND and NOR gates, respectively) show that with the increasing the number of stacked devices the gate current can increase up to 85% in NAND gate (see Table 3) and up to 98% in NOR gate of the total current value. In these tables could be seen that with the down scaling of technology the gate current increases its contribution to the total current. Finally, by analyzing the subthreshold current, one can clearly observe that the current decreases exponentially. In the Figure 3 2 it is easily seem the proportion between the gate leakage and subthreshold current in the total current.

Table 3: Gate and subthreshold current X number of stacked NMOS transistors.

	PTM_130		PTM_32	
	Igate(nA)	Isub(nA)	Igate(nA)	Isub(nA)
inv	0.110	15.90	0.283	16.70
nand2	0.228	0.896	0.602	0.524
nand3	0.346	0.647	0.922	0.343
nand4	0.464	0.566	1.24	0.291
nand5	0.581	0.525	1.56	0.267

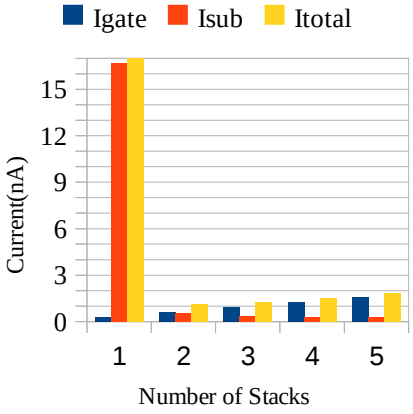

Figure 3: Evaluation of the gate leakage and subthreshold current with the stack increasing

In this last analysis the focus was to analyze a significant set of gates. To cover a good number of gates was selected the CMOS gates of 'genlib_44-6' with up to 5-inputs (about 39 gates) and other nine gates contain NSP networks. The main information of this step is which gate has the major average current, and the one (with relative input vector) which has the major maximum current. Table 4 and Table 5 present some results.

Table 4: Major average current to a given technology

	Circuit	Logic Equation	Average Current (nA)
PTM_130	circ2008	!((a * b) + (c * (d + e)))	67
PTM_65	circ1929	!(a + (b * c * (d + e)))	152
PTM_32	circ1929	!(a + (b * c * (d + e)))	57.1

Table 5: Major maximum current to a given technology

	Circuit	Logic Equation	Vector	Maximum Current (µA)
PTM_130	NSP3	e(a(b+c+d)+bcd)	10101	0.354
PTM_65	NSP7	a(b+c)+de(a+bc)	10011	0.785
PTM_32	NSP7	a(b+c)+de(a+bc)	10011	0.275

5. CONCLUSIONS

As already mentioned, to have a good idea about the static consumption of one technology it is not

enough simulate several random circuits. That is of the motivation to define a methodology in order to provide a good evaluation about the static consumption in CMOS technologies. The method proposed in this work has four well establisehd steps, which helps to organize the evaluation and simplify the comparison between technologies.

It is important to note that this analysis only cover a limited set of parasitic effects. Nowadays another static currents are becoming important, like the inverse-bias polarization current. It is indispensable to incorporate currents like that in the methodology flow, or new effects such as INWE that are present in SOI processes [10].

8. REFERENCES

[1] WESTE, N. H. E.; HARRIS, D., CMOS VLSI Design: A Circuit and Systems Perspective. PERSON, Addison Wesley, 2005.

[2] AGARWAL, A *et al.*, Leakage power analysis and reduction: models, estimation and tools. IEE Proceeding, v.152, n.3, p353-368, May 2005.

[3] B. Sheu, J. H. Shieh, and M. Patil, "BSIM: Berkeley short-channel IGFET model for MOS transistors," IEEE Journal of Solid-State Circuits, vol. SC-22, Aug. 1987. pp. 558-66

[4] W. Zhao, and Y. Cao, "New generation of predictive technology model for sub-45nm early design exploration," IEEE Transactions on Electron Devices, vol. 53, no. 11, Nov. 2006. pp. 2816-23

[5] ESCOBAR, K. A.; BUTZEN, P. F.; REIS, A. I.; RIBAS, R. P., A Test Environment for Validation of Subthreshold and Leakage Current Estimation Method in CMOS Logic Gates. SIM, 2011. p. 123.

[6] CALLEGARO, V.; MARQUES, F. S.; KLOCK, C. E.; da ROSA Jr., L. S.; RIBAS, R. P., REIS, A. I., SwitchCraft: a framework for transistor network design. Proc. SBCCI, 2010.

[7] MUKHODADHYAY, S.; RAYCHOWDHURY, A.; ROY, K. Accurate Estimation of Total Leakage in Nanometer-Scale Bulk CMOS Circuits Based on Divece Geometry and Doping Profile. IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems, New York, v.24, n.3, p. 363-381, Mar. 2005.

[8] BUTZEN, P. F.; da ROSA Jr., L. S.; CHIAPPETTA FILHO, E. J. D.; REIS, A. I.; RIBAS, R. P., Standby power consumption estimation by interacting leakage current mechanisms in nanoscaled CMOS digital circuits. Microelectronics Journal, v.4, n.4, p.247-255, Apr. 2010.

[9] ROSA JR, L. S., AUTOMATIC GENERATION AND EVALUATION OF TRANSISTOR NETWORKS IN DIFFERENT LOGIC STYLES. Ph.D. Thesis, UFRGS, Jul, 2008.

[10] PACHA, C *et al.* Impact of STI-induced stress, inverse narrow width effect, and statistical Vth variations on leakage currents in 120 nm CMOS. Proc. ESSDERC, 2004, p.397-400.

[11] YANG, S. *et al.* Accurate stacking effect macro-modeling of leakage power in sub-100nm circuits. Proc. Int'l Conf. of VLSI Design, 2005, p.165-170.

[12] E. M. Sentovich, et al., "SIS: A system for sequential circuit synthesis," Berkeley, CA: Electronic Res. Lab., Univ. California, Technica. Report. UCB/ERL M92/41, 1992

[13] CAO, K.M., et al. BSIM4 Gate Leakage Model Including Source-Drain Partition. In: INTERNATIONAL ELECTON DEVICES MEETING, 200. Digest of Technical Papers. [S.1.: s.n.], 2000. p. 815-818.