Specifications of an Integrated UHF Receiver Front-End for SBCD Satellites

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***Abstract*— This paper presents the design requirements for the front-end of an integrated UHF receiver to be embedded in satellites of the brazilian system of data collection. The uplink communication is firstly described, then the specifications of a low-IF receiver are derived. These are used to calculate the design requirements and propose suited topologies for the LNA and the mixers in a standard CMOS process.**

I. Introduction

The Brazilian System of Data Collection (SBCD) is the keystone for monitoring the huge brazilian territory through the collection of environmental data like surface temperature or atmospheric pressure. These environmental and weather informations are captured by sensors attached to Data Collection Platforms (DCP) spread all over the brazilian territory and classified as hydrological, meteorological, agro-meteorological and buoy [1]. The DCPs must packetize and send the data to low-orbit satellites through an UHF communication channel (uplink), whereas the ground station is in charge of demodulating and recovering the data received from the satellites in the range of S-band (downlink), for all the DCPs [2]. At the end of the chain, the mission control center stores and distributes the environmental data to end-users like the National Water Agency, which, for instance, uses them to monitor the water reserves through the temperature and the relative humidity.
The current transponder in the SBCD satellites is based on a super-heterodyne analog receiver shown in Fig. 1. This architecture offers an excellent sensitivity to cope with the high signal attenuation due to the large earth-space communication distance, and an excellent selectivity to reduce the susceptibility to interferers. However, the number of discrete components done with specific technologies do not allow a full-integration of this receiver into a CMOS technology, which would reduce the size, the power consumption and the cost of the system.

This paper presents the architecture and the front-end requirements of a full-integrated digitized UHF receiver for the future satellites of the SBCD system. The receiver, shown in Fig. 2, is based on a low-IF architecture to avoid the problems due to DC-offsets and $\frac{1}{f}$ noise of the zero-IF architecture [3], at the expense of a limited image rejection and a higher bandwidth for the baseband circuits [4]. In section II, we present the protocol requirements for an SBCD communication and derive, in section III, the specifications for the digitized low-IF receiver. Finally, in section IV, the proposed topologies of the low-noise amplifier (LNA) and mixers for the receiver front-end are presented with their design requirements.

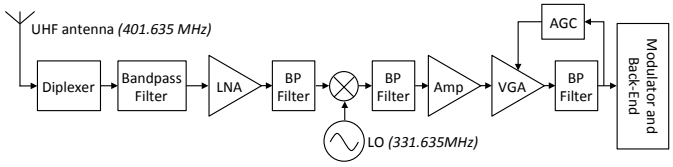

Fig. 1. Analog super-heterodyne receiver of the current SBCD satellites.

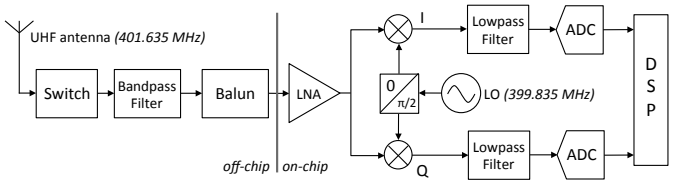

Fig. 2. Digitized low-IF receiver for the next SBCD satellites.

II. Uplink Communication Protocol

The physical data sensed by the DCPs are converted into a bit stream of 400 bps. Then, they are encoded in $biphase_L$ (Manchester), doubling the rate to 800 cps, and modulated into a $\pm 60^\circ$ binary phase shift-keying (BPSK) signal with residual carrier to enhance the detection. This modulation scheme provides a signal spectrum with a bandwidth B of 1.6 kHz containing 85% of the signal power.
The DCPs transmit to the SBCD satellites at 401.635 MHz during 360 to 920ms and with regular intervals of 40 to 220 seconds. Each satellite must be able to receive simultaneously an average of seven DCPs signals within a band of 60 kHz around 401.635 MHz [5]. The number of signals collisions are minimized due to the short duty cycle, the relative movement between the Earth and the satellites that implies a Doppler effect, and the frequency drift in time of the DCPs local oscillators. The probability of signals detection by the ground station is 95% [5], the losses being compensated by the redundancy of the signal transmissions.
Each DCP signal received by the satellite has a power level that can vary from -123 to -98 dBm to achieve a bit error rate (BER) of 0.001%. Considering the signal without the residual carrier to extract the data, the received signal power levels must be reduced by 1.25 dB (residual carrier rectification).
The main SBCD specification requirements for the satellite receiver are summarized in table I.

TABLE I

MAIN SBCD SPECIFICATION REQUIREMENTS FOR THE UPLINK RECEIVER.

Minimum Input Power	-123 dBm
Maximum Input Power	-98 dBm
Residual Carrier Rectification	-1.25 dB
Carrier Frequency	401.635 MHz
Signal Bandwidth (B)	1.6 kHz
Receiver Bandwidth (BW)	60 kHz
Bit Error Rate	10^{-5}

III. INTEGRATED RECEIVER SPECIFICATIONS

The receiver must process at the same time an average of seven DCPs signals received within a bandwidth of 30 kHz. Anyhow, the case of receiving only one DCP signal at the minimum power level exists and defines the sensitivity of the receiver. By superposition, the calculations done for one signal will be valid for seven signals, since the most powerful received signal, that defines the saturation condition, is a blocker (Fig. 3).

A. Noise Figure

From the signal modulation and the required BER, we calculate the minimum signal to noise ratio (SNR) the receiver must achieve at the analog front-end output:

$$SNR_{out} = \frac{E_b}{N_o} \times \frac{R}{B} \tag{1}$$

where E_b is the energy per bit, N_o the noise power density, R the data rate and B the signal bandwidth. The value of $\frac{E_b}{N_o}$ is 9.5 dB for a BER of 10^{-5}, the same as a classical BPSK modulation. The data rate is 800 cps and only the channel bandwidth B of 1.6 kHz is considered here, not the entire 60 kHz (BW), since the demodulation is done after having digitally extracted each channel of 1.6 kHz within the 60 kHz band. We add 1 dB as margin on the digital signal processing and 2 dB to compensate the power loss due to the band of 1.6 kHz and the residual carrier rectification. Hence, the minimum output SNR is:

$$SNR_{out} = 9.5 + 10\log_{10}\left(\frac{800}{1600}\right) + 1 + 2 = 9.5\ dB \tag{2}$$

The minimum power of the desired signal at the LNA input is derived from the minimum power received attenuated by the discrete components losses: switch (0.5 dB), cables (0.5 dB), UHF filter (1 dB) and balun (1.5 dB):

$$P_{in,min} = -123 - 3.5 = -126.5\ dBm \tag{3}$$

The noise floor at the LNA input is due to the impedance matching at the chip interface and thus depends on the receiver temperature, which varies between -10 to $50\,^{\circ}$C. In order to design a robust receiver we consider the worst case, when the temperature is the highest. In this case, the noise floor is:

$$Noise\ Floor = 10\log_{10}\left(\frac{k \times T \times B}{0.001}\right) = -141.5\ dBm \tag{4}$$

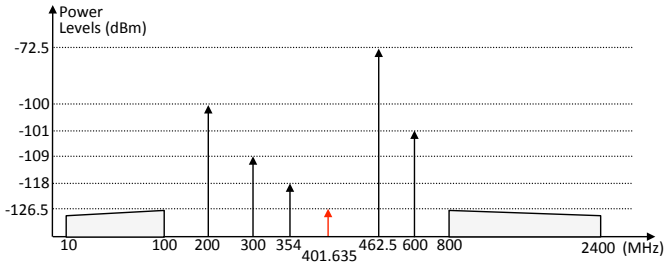

Fig. 3. Desired signal at 401.635 MHz and blockers signals at the LNA input.

Finally, we can calculate the SNR at the LNA input and then derive the Noise Figure (NF) that gives the noise budget for the receiver design:

$$\begin{aligned} NF &= SNR_{in} - SNR_{out}\ (dB) \\ &= [-126.5 - (-141.5)] - 9.5 = 5.5\ dB \end{aligned} \tag{5}$$

B. Gain

The gain of the receiver front-end is calculated to scale the minimum signal power $P_{in,min}$ to the minimum level in the dynamic range of the analog-to-digital converter (ADC) that respects SNR_{out}. Considering the ADC with the specifications given in table II, its input referred noise level is calculated as:

$$ADC_{noise} = 0 - 14 \times 6.02 + 1.76 = -86\ dBm \tag{6}$$

A design choice is to neglect the ADC noise regarding the noise power added by the previous blocks. Hence, we consider a margin of 10 dB (ADC_{margin}) between the front-end noise and the ADC noise. This leads to determine the required gain G for the receiver front-end with the following expression:

$$\begin{aligned} G &= ADC_{noise} + ADC_{margin} + SNR_{out} - P_{in,min} \\ &= -86 + 10 + 9.5 - (-126.5) = 60\ dB \end{aligned} \tag{7}$$

C. Selectivity

The satellite receiver must process two types of blockers: narrow-band (tone) and wide-band, as illustrated in Fig. 3. They are first filtered by the off-chip UHF filter before reaching the LNA input with the power levels given in Fig. 3. The on-chip filtering is split between the analog filter and the digital filters. The analog filter is used to limit the power of the blockers aliased into the signal band after the ADC sampling, and the digital filters are used to remove the remaining out-of-band blockers. The ADC sampling frequency determines where the blockers will be aliased and thus the specifications

TABLE II

PART OF THE ADC SPECIFICATIONS FOR A BANDWIDTH OF 1.6 KHZ.

Resolution	14 bits
Reference Level	0 dBm
Noise Margin (ADC_{margin})	10 dB

of the filters. Considering a lowpass oversampled ADC, its sampling frequency is defined in a low-IF receiver as:

$$f_{samp} = OSR \times 2 \times \left(f_{IF} + \frac{BW}{2} \right) \quad (8)$$

where OSR is the ADC oversampling ratio fixed on 32, f_{IF} is the receiver intermediate frequency and BW is the receiver bandwidth of 60 kHz. From equ. (8) we can see that only f_{IF} determines the ADC sampling frequency. Hence, for different f_{IF} frequencies we are able to calculate the corresponding ADC sampling frequencies and derive the frequencies of the narrow-band blockers aliased after the ADC sampling. We did not consider the wide-band blockers since they will alias inevitably into the signal band, but have power levels much lower than the narrow-band blockers and thus are not critical for the choice of the ADC sampling frequency.

Then, we apply to the narrow-band blockers the gain G previously determined and list their frequencies and power levels after the ADC sampling in the table III. From this, we deduce that the low-IF frequency giving the most relaxed specifications for the analog and digital filters is:

$$f_{IF} = 1.8\ MHz$$

In this case, the blockers in the vicinity of the signal have the lowest power levels and the blocker with the highest power level (-12 dBm) is far (54 MHz) from the bandwidth edge (1.83 MHz). The corresponding ADC sampling frequency f_{samp} is 117.12 MHz. System simulations are shown in Fig. 4 and confirm the blockers frequencies after the ADC sampling. In this case, we use a third order lowpass filter to relax the linearity requirement for the ADC, remove the wide-band blockers and highly attenuate the noise that alias into the signal band.

By defining the IF frequency (1.8 MHz) we define at the same time the image frequency (398.035 MHz) where there is no blocker defined. Anyhow, to design a robust receiver we need to achieve at least 30 dB of image rejection. Using the formula defined in [4], we calculate a maximal difference in phase of 3° and in gain of 3% between the in-phase and quadrature-phase signals.

D. Linearity

Since the blockers are widely spread on the frequency spectrum, there is no significant intermodulation products. On the other hand, due to the high power of the blockers in comparison with the signal, we need to consider the 1 dB compression point (CP1) in order to avoid the saturation of the front-end blocks. We take a margin of 3 dB above the power level B_{in} of the strongest blocker at the front-end output to define the output CP1:

$$OCP_1 = B_{in} + G + 3 - 1 = -72.5 + 60 + 2 \simeq -10\ dBm \quad (9)$$

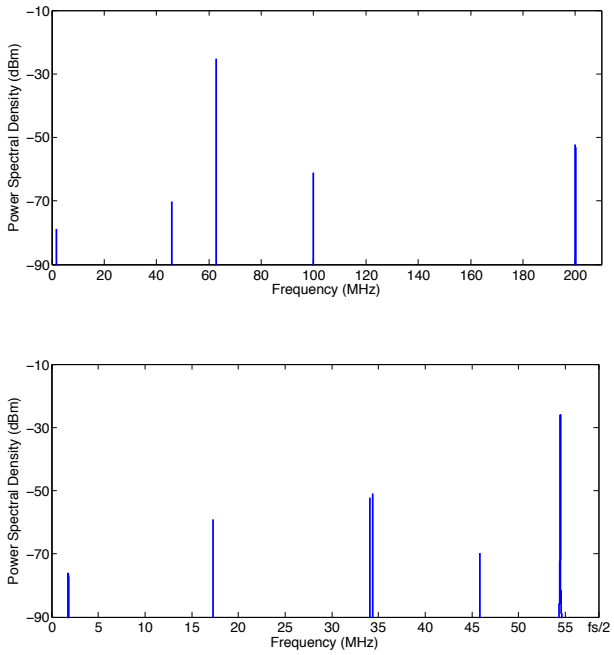

Fig. 4. top: spectrum of the signal downconverted to f_{IF} =1.8 MHz and narrow-band blockers - bottom: spectrum of the signal and narrow-band blockers after the ADC sampling with f_{samp}=117.12 MHz.

IV. UHF Front-End

A design choice is to implement the overall receiver gain in the UHF front-end, which has its requirements summarized in table IV. In this way, the NF is also totally specified for the UHF front-end since the noise of the subsequent stages will be negligible. From these requirements we derive in the following subsections the specifications and suited topologies for the LNA and the mixers.

TABLE III
FREQUENCY AND POWER OF BLOCKERS AFTER THE ADC SAMPLING.

Low-IF		Bl 1	Bl 2	Bl 3	Bl 4	Bl 5
1.1 MHz	MHz	9.655	16.795	17.125	26.485	27.515
1.1 MHz	dBm	-12	-41	-39	-57	-49
1.3 MHz	MHz	14.715	22.455	29.595	29.925	39.285
1.3 MHz	dBm	-49	-12	-39	-41	-57
1.8 MHz	MHz	17.285	34.075	34.405	45.835	54.455
1.8 MHz	dBm	-49	-41	-39	-57	-12
2.6 MHz	MHz	31.515	31.845	45.835	62.665	68.485
2.6 MHz	dBm	-39	-41	-57	-12	-49

TABLE IV
UHF FRONT-END REQUIREMENTS.

Sensitivity	-126.5 dBm
Maximum Input Power	-101.5 dBm
Carrier Frequency	401.635 MHz
LO Frequency	399.835 MHz
Receiver Bandwidth	60 kHz
Gain	60 dB
NF	5.5 dB
OCP1	-10 dBm
I/Q phase difference	3°
I/Q gain difference	3%

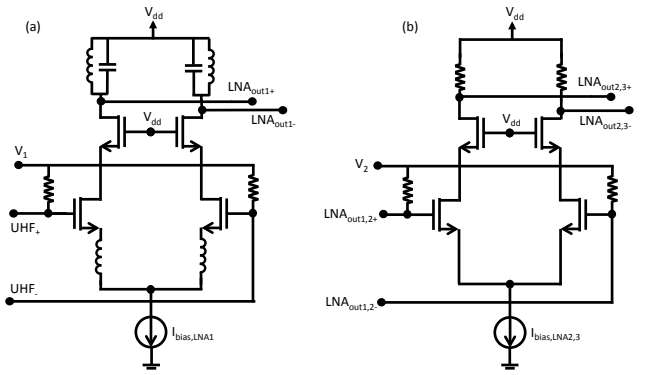

Fig. 5. The multiple-stages LNA: the first stage (a), the second and third stages (b).

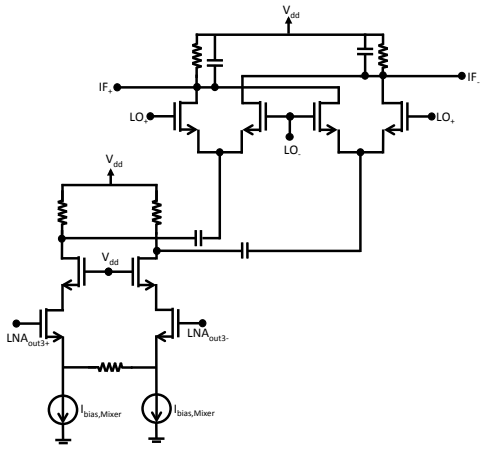

Fig. 6. The passive mixer with its input buffer.

A. Low-Noise Amplifier

The gain of 60 dB is realized using an LNA with three stages [6]. Each stage has a gain of 20 dB. The first stage (Fig.5 (a)) is the most critical, because it must realize the impedance matching to maximize the power delivered into the chip ($S_{11} < -10$ dB), and amplify the signal with a small NF to relax the constraints on the noise for the subsequent stages. A typical common source topology is used with cascoded transistors to drastically reduce the Miller effect, and an inductive degeneration to present a 50 Ω input impedance. A low-noise LC tank loads the stage and slightly attenuates the blockers. Due to size issues, the second and the third stages (Fig.5 (b)) have an inductorless cascode topology with a resistive load. Their induced noise is higher, but its effect is reduced by the gain of the first stage. In table V we summarize the LNA specifications.

B. Mixers

The mixer has the function of translating the signal from the UHF band at 401.635 MHz to the low-IF frequency of 1.8 MHz. Due to the limited NF and the stringent requirements on the linearity (table VI), we use a passive mixer [7] which is ideally noiseless and linear (Fig. 6). The conversion losses of this topology are compensated by using a buffer at the mixer input [8]. The buffer adds noise and non-linearity but, with a cascode structure, helps to isolate the LNA from the varying mixer input impedance. The conversion gain is determined by the buffer transconductance, the coupling capacitor, the switches R_{on} and the first filter stage that loads the mixer. The requirements to guarantee the specified image-rejection ratio must be validated through the good matching of the in-phase and quadrature-phase mixers.

TABLE V

LNA REQUIREMENTS.

Input Signal Frequency	401.635 MHz
NF	$<$ 5.4 dB
Gain $1^{st}/2^{nd}/3^{rd}$	20 dB / 20 dB / 20 dB
S_{11}	$<$ -10 dB
OCP1	$>$ -10 dBm

TABLE VI

MIXER REQUIREMENTS.

LO Frequency	399.835 MHz
Conversion Gain	0 dB
iCP1	$>$-9 dBm
I/Q phase difference	3°
I/Q gain difference	3%

V. CONCLUSION

In this paper we presented the specifications of an integrated UHF low-IF receiver derived from the requirements of the brazilian system of data collection. The critical choice of the intermediate frequency has been done in relation with the ADC specifications to avoid an SNR degradation or a complex digital filtering. This has been validated through system simulations and lead to define the requirements for the baseband analog filter placed before the ADC. Finally, we proposed LNA and mixer topologies to cope with the challenging front-end receiver specifications in terms of gain and noise.

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