UCAF – A FRAMEWORK FOR ANALOG INTEGRATED CIRCUIT ANALYSIS AND DESIGN

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ABSTRACT

This paper presents a fully configurable framework for analog integrated circuit design automation. The goal of this framework, named as UCAF, is to provide in a single environment several optimization heuristics, design methodologies and technology options in order to allow for the designer the possibility to perform a set of comparisons and selections aiming the optimized design.

UCAF was implemented in Matlab® and has a friendly graphical interface (GUI) for input and output.

As results and examples of use we present the design automation of a Miller Operational Transconductance Amplifier (OTA), comparing design objectives and fabrication processes.

1. INTRODUCTION

Design automation of analog integrated circuits is a demanding task in microelectronics industry because of the crescent necessity for low-power and reduced time-to-market, which requires an efficient design space exploration for finding optimized design solutions.

Typically, most of analog integrated circuit designs are done manually – with some aid of simulation tools and equation-based models - and the quality of the resulting circuit is dependent on the expertise of the designer. A system-on-chip (SOC) design can have analog and digital parts in the same die, each one designed with different methodologies and tools. The analog design time must be compatible with the highly automated digital design time, which employs advanced design automation tools [1].

According to Graeb [2], about 75% of the integrated circuits (ICs) have analog parts. In these ICs, about 20% of the area is occupied by the analog parts, but these parts demand about 40% of the overall design effort. Moreover, analog parts are responsible to 50% of the design defects. Two main causes of this are the complexity of analog circuit design and the lack of design automation tools. According to Hägglund [3], Computer-Aided Design (CAD) and Electronics Design Automation (EDA) tools growing are not following the CMOS technology evolution, creating a design gap, as shown in Figure 1. Thus, the development of analog design tools is very important to design circuit with high productivity, reliability and low time-to-market.

The design of analog integrated circuits can be divided in 3 steps: topology selection, transistor sizing and layout generation. This paper will focus on the second step, which is critical for achieving the desired circuit performance under a set of constraints.

The design space for the automatic synthesis of analog CMOS integrated amplifiers is highly nonlinear. There are about ten free variables in a typical operational transconductance amplifier design, related to gate dimensions - width (W) and length (L) -, bias currents and inversion levels.

As the relation between transistor sizes and circuit specifications (design objectives) is nonlinear and sometimes conflicting, the problem of finding an optimum solution point is difficult to be exactly solvable and it usually must be approximated by analytical or numerical analysis. Some previous works have been done in this theme describing the development of tools for analog design automation (ADA). The goal is always the automation of time-consuming tasks and complex searches in highly non-linear design spaces [4][5]. Different automatic design strategies have been proposed, using different meta-heuristics and algorithms [6][7]. Basically all of them can be categorized as equation-based or simulation-based automatic designs. In the equation-based design strategy, analytical equations are used for modeling device electrical characteristics, such as drain current, inversion level and small-signal parameters. These models are often simplified or manipulated in order to fit certain limitations imposed by optimization heuristics. The simulation-based strategy is based on the result of the electrical simulation of the circuit to extract device parameters and design characteristics. The simulation can be automated and performed several times until reaching the design objective.

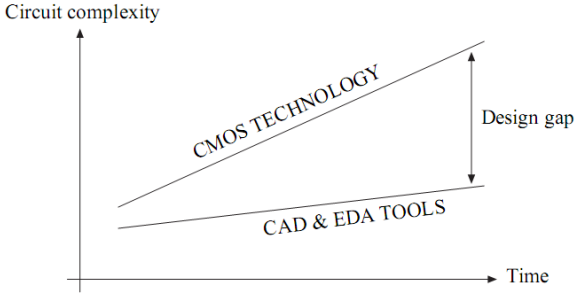

Figure 1 – The increase in circuit complexity compared to the productivity growth rate due to CAD and EDA tools [3].

Based on the demand for analog integrated circuit design tools, this paper has the goal to present a framework, named as UCAF, capable to analyze and design basic analog blocks. UCAF allows the

configuration of a series of design options. Thus, it is possible analyze the results and make comparisons of automatic design using a variety of functions and configurations, as, for example, different optimization heuristics, fabrication technologies and circuit topologies.

As design example, this paper presents the sizing procedure of a power and area constrained design of a two-stage CMOS Miller operational transconductance amplifier (OTA), considering different design specifications and fabrication technologies.

2. UCAF ANALOG INTEGRATED CIRCUIT FRAMEWORK

This work proposes a fully configurable tool for analog integrated circuit design automation, aiming to be a framework integrating several design strategies. The tool, named as UCAF, is implemented in Matlab. The general design flow is shown in Figure 2. The tool receives as input an initial design solution, design requirements and fabrication technology parameters. These information are the inputs of the optimization heuristic algorithm, which, based on the free variables bounds, generates an optimized solution for the circuit.

To analyze the quality of the generated solution it is used a cost function, which is calculated based on the specifications obtained by electrical simulation.

UCAF is composed by an user-friendly input interface used to configure the design procedure and an output graphical interface used to analyze the execution results. These interfaces are linked to the core of the tool, which contains modular functions implemented in order to automate the design, as shown in the Figure 3. The modular functions are described in next subsections.

2.1. Technology

It is used to setting the tool with the transistor model and the technology parameters. Several transistor models are supported, such as BSIM3v3, ACM, EKV, etc, depending on the electrical simulator tool to be used. The fabrication process is also configurable and must be informed by the user.

2.2. SPICE Simulator

This module selects the third-part SPICE electrical simulator to be used to analyze the results of a generated solution. The framework does not have a built-in electrical simulator, but it can automatically interface with a series of SPICE simulators.

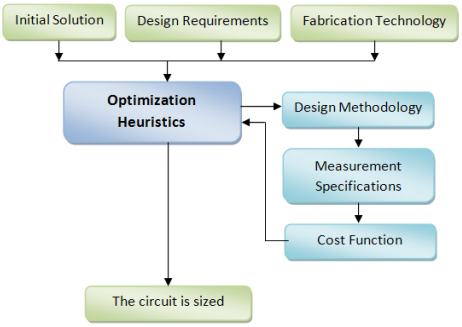

Figure 2 – Analog circuit design automation tool.

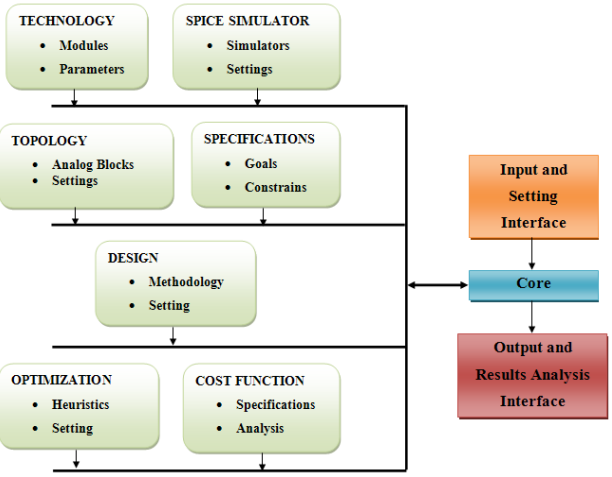

Figure 3 – Framework block diagram.

2.3. Topology

The topologies are the circuits that are available in the framework for optimization. In general they are basic analog building blocks, such as current mirrors, amplifiers and comparators. As the UCAF framework is composed by modular functions, it is easy to insert new topologies in the tool environment.

2.4. Specifications

In this module the user sets the specifications values and the optimizations goals of the design, indicating the minimum and maximum values. The user also must inform which are the design objectives and the design constraints.

2.5. Design

This module is used to size the MOSFET transistors. In other words it is the form to convert the optimization free variables in the transistor sizes. In the current version of UCAF there are available two methodologies: Direct and gm/I_D. These methodologies are shown in the Figure 4.

In the Direct Methodology the optimization heuristic has as free variables the transistor dimensions W and L. In the gm/I_D Methodology it is used the design technique proposed by [8] and the optimization heuristic has the transistor lengths (L) and the gm/I_D values as free variables. Based on the circuit specifications and on the gm/I_D vs I_N (normalized current) curve, the transistor sizes are obtained.

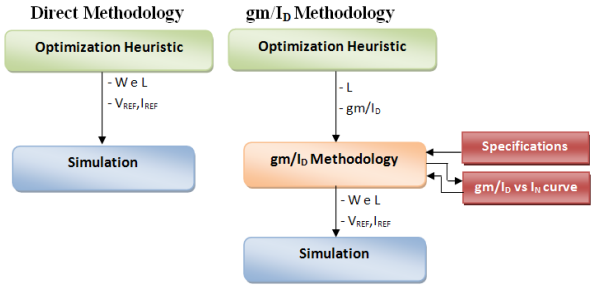

Figure 4 – Design methodology.

2.6. Optimization

The user can select the optimization heuristic to be used to explore the design space for finding optimized solutions that met design constrains. Two heuristics are implemented: Genetic Algorithms and Simulated Annealing. We used the GAOT [9] for genetic algorithm and ASAMIN [10] for simulated annealing.

2.7. Cost Function

The optimization process uses a cost function to evaluate the generated solution. This function is a multi-objective function, in the format of the Equation 1, where the first sum is formed by the design specifications to optimize (E_i) and the second sum is formed by normalized values of design constraints. The value of $V(E_J)$ is equal to zero for a specification that met the required value or positive if otherwise. P_{Oi} and P_{Rj} are the weighting values for design objectives and design constraints, respectively.

$$f_c = \sum_{i=1}^{n} P_{O_i}.E_i + \sum_{j=1}^{n} P_{R_j}.V(E_j) \quad (1)$$

3. DESIGN AND ANALYSIS OF RESULTS

As a design example using the proposed UCAF framework, described in this paper, we used a two-stage CMOS Miller operational transconductance amplifier (OTA). The schematic of this amplifier is shown in Figure 5. The Miller OTA is composed by an input differential pair and a current mirror with active load in the first stage. The second stage is composed by an inverter amplifier. Between the first and second stages is connected a compensation capacitor for stability purposes [11].

The main specifications of this circuit are low frequency gain (Av_0), slew rate (SR), phase margin (PM), input common-mode range (ICMR), output swing (OS), power consumption and gate area.

3.1. Specifications Analysis

For this design example we used the parameters of the AMS 0.35µm technology extracted to ACM model [12], the Smash® simulator, the gm/I_D methodology and the Genetic Algorithms heuristics. In this design the goal is minimize the power dissipation and the gate area of the circuit.

Table 1 shows the required specifications in the three different designs and Tables 2 and 3 shows the results of this analysis. Analyzing the results it is possible to notice that all specifications values are met. The power dissipation increase with the increasing of SR and GBW requirements, which is expected because these specifications are proportional to the consumed electrical current, proportional to power dissipation.

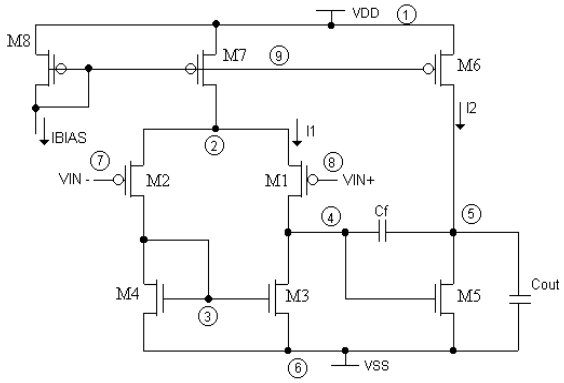

Figure 5 - Schematics of a two-stage Miller operational transconductance amplifier.

In Table 3, obtained values of gm/I_D for transistors M1, M5 and M6 are presented. They are inversely proportional to the inversion level. It can be verified that the inversion levels of transistor M1 and M6 increase with SR and GBW specifications.

3.2. Technology analysis

In this design results the goal is to analyze the design of an OTA Miller in two different technologies: AMS 0.35µm and XFAB 0.18µm.

The UCAF framework was setting to use the Smash® simulator, Simulated Annealing heuristic, direct methodology and used the same specifications values for both technologies. The goal of optimizations is minimize the power dissipation and the gate area.

The required values as well as the reached values are shown in the Table 4. In these results it is possible to see that all specifications required are met. Analyzing the best result, minimum power dissipation and gate area, is possible see that the best result is obtained with the XFAB 0.18µm technology. In the best result were found the power dissipation about 45% less than AMS 0.35µm technology and the gate area of the circuit about 80% less than 0.35µm technology.

The reached result is justified because the XFAB 0.18µm has smaller transistor sizes and voltage supply, these specifications are important to find circuit with reduced size and low power dissipation.

Table 1 – Design specifications of the three designs

Specification	Design 1	Design 2	Design 3
Avo (dB)	≥ 70	≥ 70	≥ 70
GBW (MHz)	≥ 0.10	≥ 1	≥ 10
PM (°)	≥ 60°	≥ 60°	≥ 60°
SR (V/µs)	≥ 0,1	≥ 1	≥ 10
ICMR+ (V)	≥ 0,7	≥ 0,7	≥ 0,7
ICMR- (V)	≤ -0,7	≤ -0,7	≤ -0,7
Pdiss (µW)	↓	↓	↓
Gate area (µm²)	↓	↓	↓

Table 2 – Design results of the three designs

Specification	Design 1	Design 2	Design 3
Avo (dB)	73,50	70,10	76,00
GBW (MHz)	0,1	1,0	10,00
PM (°)	63	60,8	98,1
SR (V/µs)	0,1	0,99	9,9
ICMR+ (V)	1,3	1,35	1,31
ICMR- (V)	-1,64	-1,60	-1,64
Pdiss (µW)	3,52	58,20	296,01
Gate area (µm²)	740,8	502,5	6678,3

Table 3 – Variables values of the three designs

Specification	Design 1	Design 2	Design 3
W1 (µm)	1,81	4,19	320,18
L1 (µm)	1,31	0,44	10,01
W3 (µm)	19,80	10,21	54,80
L3 (µm)	9,92	3,48	0,43
W5 (µm)	47,60	100,02	186,90
L5 (µm)	3,62	3,75	0,37
W6 (µm)	9,96	3,74	7,10
L6 (µm)	15,71	5,50	11,30
W7 (µm)	1,32	1,61	4,11
L7 (µm)	5,51	10,00	9,94
(gm/ID)1	17,52	15,20	10,30
(gm/ID)5	23,50	14,15	22,73
(gm/ID)6	6,69	1,73	0,56

Table 4 – Design results of the technology Comparison

Specifications	Required	XFAB 0.18µm	AMS 0.35 µm
Av_0 (dB)	≥ 70	85.71	73.88
GBW (MHz)	≥ 1	1.80	1.14
PM (°)	≥ 60°	72.35	85.87
SR (V/µs)	≥ 1.00	1.00	1.02
ICMR+ (V)	≥ 0.4	0.62	1.30
ICMR – (V)	≤ -0.4	-0.87	-1.62
OS+ (V)	≥ 0,8	0.82	1.50
OS- (V)	≤ -0.8	-0.89	-1.64
Pdiss (µW)	↓	18.05	33.00
Gate Area (µm²)	↓	108.39	546.21
Iterations	-	1572	2292
Execution time (min)	-	52.0	45.0

4. CONCLUSION

In this paper a framework for fully configurable automatic analog integrated circuit design and analysis, named as UCAF, is presented. With UCAF framework it is possible to analyze and configure the fabrication technology, optimization heuristics, sizing methodology and circuit topologies.

Two design examples of an OTA Miller were presented. In this designs were compared the results for three set of design specifications and two different fabrication technologies, all with optimization of the gate area and power dissipation.

The design results show that with the UCAF framework is possible to analyze and design analog integrated circuits in several configuration profiles.

As future work we intend to insert new circuit topologies in the framework, insert a parameter variation analysis and fabricate circuits designed with the tool for physical validation.

5. ACKNOWLEDGMENTS

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