DESIGN METHODOLOGY OF ANALOG INTEGRATED CIRCUITS USING CARBON NANOTUBE TRANSISTORS

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ABSTRACT

This work aims to present a proposed design methodology of analog integrated circuits composed entirely by carbon nanotube transistors (CNTFETs). The application of carbon nanotube transistors in analog circuits is incipient nowadays and a methodology for this type of design is not well defined. The proposed methodology is based on the translation a CMOS design for an equivalent CNTFET design with the same bias point. For validation and testing of the proposed methodology this paper presents the design of a differential amplifier. Some comparisons are made so that the advantages and disadvantages of this methodology can be analyzed.

1. INTRODUCTION

With the evolution of integrated circuits, there is a need to reduce the size of transistors to address the growing demand for equipment with higher speed and lower power consumption. Nowadays, the CMOS integrated circuit technology is dominant over other manufacturing technologies. However, CMOS technology will reach a point where the physical dimensions will be limited to restrictive factors for the evolution of the manufacturing process of transistors.

Thus, it is necessary to constantly search for new alternatives to replace or complement the CMOS technology, in order to obtain circuits with less power consumption, higher speed and smaller size. However, to achieve faster circuits, it is necessary to design transistors with better capacity to drive current. To this end, a strong replacement candidate for CMOS technology, or additive to this technology, is the carbon nanotube technology, which can be used for the fabrication of transistors with speed 10 to 100 times faster than CMOS technology [1].

Therefore, this paper proposes a design methodology for analog integrated circuits using carbon nanotube transistors. For CMOS technology, design methodologies are well consolidated. These methodologies address a series of steps in which the initial solution of a design can be estimated by simplified design equations. Thus, by means of simple equations it is possible to obtain a first version of the circuit. Using electrical simulators, the parameters are adjusted to improve the specifications required by the circuit. In this context, analog circuit design using CNTFET technology is a challenge, since due to its characteristics, the traditional CMOS design methodology cannot be directly adopted, motivating the development of new strategies and techniques.

Next sections describe the proposed methodology, which is validated with the design of a simple differential amplifier whose electrical simulations are presented.

2. CARBON NANOTUBES AND THE CNTFET

The theory of carbon nanotubes (CNTs) was first described by Ijima in 1991 [2], and is still in its early stage of development [3][4].

Carbon nanotubes are hollow cylinders composed by one or more concentric layers of carbon atoms similar to a honeycomb lattice. They can be produced from a sheet of graphene rolled up, producing perfect cylinders.

The CNT's are divided into two categories: (i) single-wall nanotubes and (ii) multi-wall nanotubes [2][8]. Figure 1 illustrates both categories.

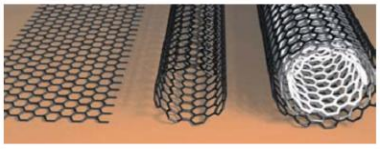


FIGURE 1 - Illustration of a sheet of graphene (left), single-wall nanotube (middle) and multi-wall nanotube (right) [8].

Electrical characteristics of a nanotube are defined according to the direction the graphene sheet is rolled up. The chiral vector is defined by the following equation:

$$C_h = na_1 + na_2 \quad (1)$$

Here, a_1 and a_2 are the unit vectors of the graphene lattice, and n and m are integers.

According to the chiral vector, the nanotube receive special denomination: if n=m, it is called armchair; for (n,0) pairs the nanotube is called zigzag; otherwise it is called chiral. This characteristic defines if the device will be a conductor or a semiconductor. The diameter D is also dependent on the chiral vector and can be calculated as:

$$D = a.s\ \sqrt{n^2 + m^2}\ + (n.m)/\pi \quad (2)$$

In this work, we used the zigzag type nanotube, with n=19 and m=0, which has semiconducting electrical characteristics and diameter of 1.5089 nm.

One of the main promising uses of carbon nanotubes in microelectronics is for the fabrication of carbon nanotube field effect transistors (CNTFETs). The structure of a CNTFET is composed by three terminals:

gate, drain and source. As it is build over an isolation, the bulk terminal is not part of the intrinsic device. The designation of the terminals is identical to a CMOS transistor due to the fact that both have the same constructive form. The channel region of a CMOS transistor is replaced by a carbon nanotube connecting drain to source, as shown in Figure 2.

(a) (b)

FIGURE 2 - Illustration of a CMOS structure (a) and CNTFET (b).

So, analyzing an N-type CNTFET, when a positive potential difference is applied in the gate terminal, there is a current flowing from drain to source if there is a positive potential difference between drain and source [7] [8]. In CNTFETs a quasi-ballistic transport of carriers occurs (due to the carbon nanotube structure), resulting in a higher electrical current.

3. EQUIVALENCE BETWEEN CMOS AND CNTFET

For CMOS technology, the designer of analog integrated circuits in general has the following free variables: W (channel width) and L (channel length). However, for the CNTFET technology, the channel width is fixed (equal to the diameter of a nanotube) and the free variables are L and the number of nanotubes in parallel (N).

In a CMOS transistor the channel width (W) can be varied continuously, limited by the resolution of the manufacturing technology. In the CNTFET technology, the channel width is given by the number of carbon nanotubes that connect the source and drain region in parallel. Thus, W can be sized in discrete steps, dependent on the number of nanotubes that the transistor is formed.

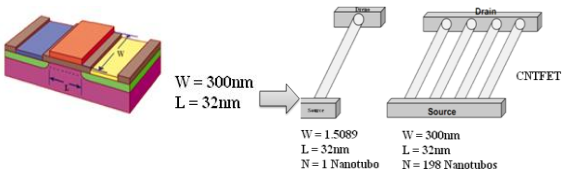


FIGURE 3 – Equivalence between the CMOS and CNTFET.

We can calculate an equivalence between both technologies. Taking as basis a CMOS transistor with W=300nm and L=32nm, we can estimate an equivalent CNTFET with the gate composed by a parallel association 198 nanotubes, each with 1.51nm individual diameter and L=32nm, as show in Figure 3. This geometrical equivalency, however, does not means electrical equivalence, as will be seen in the next section.

4. DESIGN METHODOLOGY

The design of analog integrated circuit in CMOS technology in general is based on simplified equations that model the behavior of the circuit. So it is possible to relate the characteristics of the circuit (specification) with the size of each transistor. From these equations it is possible to obtain an initial solution for the circuit. This initial solution, in general, does not reach all the necessary specifications of the circuit as, for example, minimum voltage gain, response speed, among others. The specifications of the circuits are analyzed using electrical simulation, which makes use of models, whose approach to the real world is often better than the simplified design equations. Based on the results of electrical simulation, the designer can accurately determine the value of the specifications of the circuit. If some specification does not reach the required value, the size of the transistor should be fine-tune in order to obtain a circuit solution that meets the minimum requirements.

The design with CNTFET cannot use the same approach, because the equations describing the electrical behavior of the device are not suitable for hand calculations, being necessary the use of computational tools for finding the L and the number of parallel nanotubes for each transistor that meet the required circuit specification.

An alternative, describe in this paper, is the translation of the CMOS design for an equivalent CNTFET design. This methodology starts with a pre-validated CMOS design, with all Ws an Ls known, and transcription to a CNTFET version, in which each transistor has the same original bias point.

The flowchart of this methodology is shown in Figure 4, where the first part refers to the circuit design in CMOS technology, as explained above.

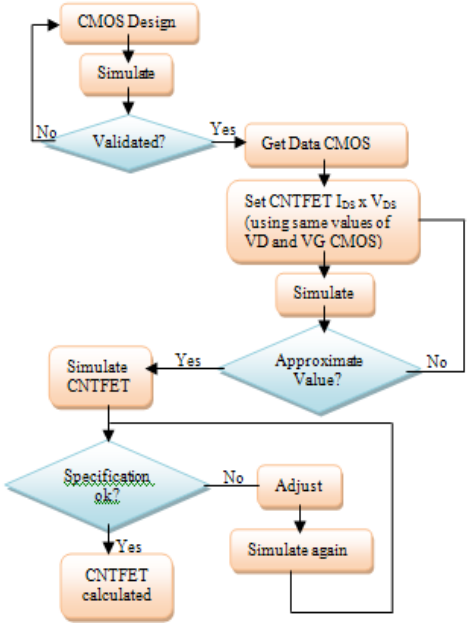


FIGURE 4 - Flowchart of the proposed methodology.

After the design in CMOS technology, the bias point of each transistor is extracted (gate-source voltage (V_{GS}), drain-source voltage (V_{DS}) and bulk-voltage source (V_{BS}) and used as reference to find an equivalent CNTFET with the same current level for these conditions.

Based on these values, the simulation is performed for the extraction of characteristic curves I_{DS} x V_{DS} and I_{DS} x V_{GS} for each CMOS transistor, where the goal is to observe the bias point of the devices. After this step, the electrical simulation of I_{DS} x V_{DS} and I_{DS} x V_{GS} for CNTFETs with different L and N is executed, adopting the same values of V_{DS} and V_{GS}.

Plotting in the same graph the results obtained for a single CMOS transistor and some CNTFETs with different N and L, it is possible to observe the equivalence point and to extract the parallel association of nanotubes that match the desired equivalency. FIGURE 5 shows an example of I_{DS} x V_{DS} curve for a CMOS transistor and for three CNTFETs with fixed L and different values of N. When looking at the graph, it is possible to notice that the CNTFET current increases with N in the saturation region.

In this example, the green curve (N=4) is very close to the bias point of the CMOS transistor and it is the best solution compared to the curves of CNTFETs with N=3 and N=5. As can be seen in Figure 5, the blue curve represents the current of a CNTFET with 3 nanotubes and the red curve for one with 5 nanotubes. Thus, it is possible to verify that the variation in the saturation current of a CNTFET is discrete, depending on the integer number of individual nanotubes. So, in some cases it would not be possible to approach the operating point of a CMOS transistor with a CNTFET.

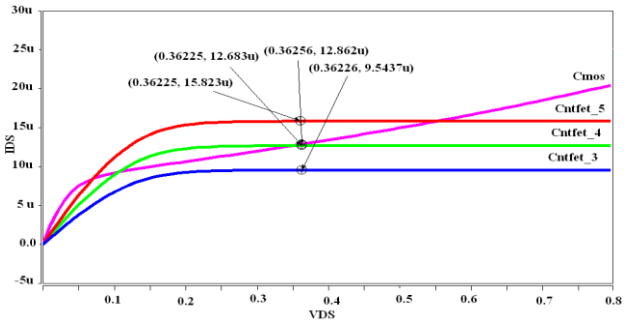


FIGURE 5 – Curve I_{DS} x V_{DS} for CMOS technology and CNTFET (distinct values of n).

Performing this procedure for all the transistors that compose a given analog circuit, it is possible to estimate all the dimensions of the circuit with CNTFET, maintaining the same bias point of the circuit.

Obviously, the small signal characteristics of the distinct technology devices are different, even for the same large signal bias point. Following the proposed methodology flow, it is necessary to re-simulate the circuit with CNTFETs using the values obtained in the previous step in order to estimate the design specifications and the electrical behavior of the hole circuit. If the simulations show that the circuit achieve the design specifications, the CNTFET design is ready. Otherwise, if the specifications are not met, the designer must perform some adjustments by varying N and L of the transistors that most influence the required specification. So, the translation procedure gives an initial CNTFET design that, in general, is very close to the final circuit. The fact that a specification is not achieved by the initial design is explained by the fact that not even a perfect translation is possible, mainly because the discrete N value. Thus, the operating point is not the same and the designer need to make some adjustments until both technologies have the same bias point.

5. DESIGN OF A DIFFERENTIAL AMPLIFIER

In order to exemplify the proposed methodology, this section presents the design of a CMOS differential amplifier and the correspondent translation for the CNTFET design. The technology used was 32nm predictive model for CMOS [9] and CNTFET [10]. The electrical simulator HSPICE ® was used for electrical simulations and the CosmoScope® tool for waveform generation.

The differential amplifier is an analog integrated circuit that has numerous applications. The operation of this circuit is given in order to amplify the voltage difference between its inputs. Figure 6, presents the schematic of the differential amplifier.

The differential amplifier comprises a differential pair (M1 and M2), a current mirror active load (M3 and M4) and a reference current mirror (M5 and M6). The main circuit specifications are: low frequency voltage gain (Av0), slew rate (SR), gain-bandwidth product (GBW) and input common mode voltage range (ICMR). Designer free variables are W1, L1, W3, L3, W5, L5 and I_{ref}.

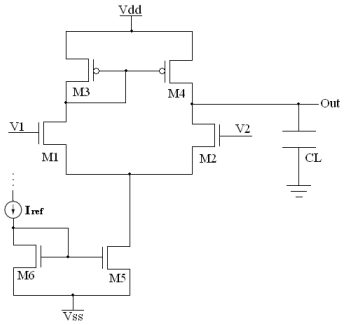
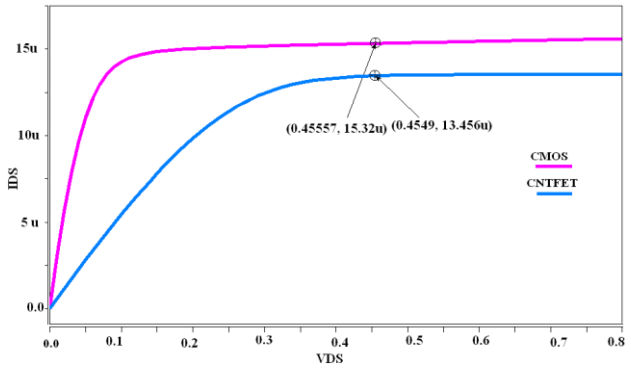


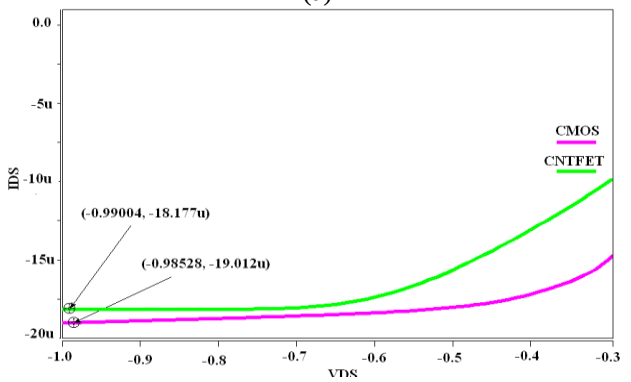
FIGURE 6 - Schematic of a differential amplifier

To perform the design of the CMOS differential amplifier, the first step is to verify the design specifications and then, using an equation-based methodology [6], size the transistors according to this specifications. After that, based on electrical simulation, the specifications of the circuit are evaluated. If the specifications required values are reached, the circuit is designed. Table 1 shows the specifications of the CMOS differential amplifier. We achieved the dimensions shown in Table 2 to technologies CMOS and the electrical specifications are shown in the third column of Table 1 to CMOS. Applying the proposed methodology described

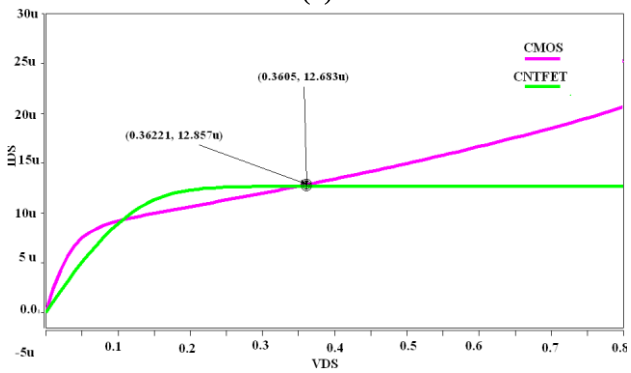
in this work, the differential amplifier is designed for CNTFET technology. Figure 7 shows I_{DS} x V_{DS} characteristics for M1, M3 and M5, with the indication of the bias point in the CMOS design. It is possible to notice that the equivalence of CNTFETs are very close in the bias point. The resulting specifications for the CNTFET design are show in the fourth column of Table 1 and the dimensions of nanotubes are show in Table 2. We can see that all specifications were met by CNTFET design with this direct translation. Also, some specifications presented better results than the CMOS design, such as low voltage gain and slew rate.



(a)



(b)



(c)

FIGURE 7 – I_{DS} x V_{DS} curve for CMOS and CNTFET technology, with the indication of the design bias point. (a) M1; (b) M3; (c) M5.

6. CONCLUSION

In this paper we proposed a methodology for sizing CNTFET transistors based on a previously sized circuit in CMOS technology. The proposed methodology proved to be valid since the results obtained by the CNTFET technology design achieved the same or better specifications as the CMOS design. This is a promising alternative for future analog integrated circuit design with carbon nanotubes compatible with traditional CMOS design methodology.

Table1 - Differential CMOS Amplifier Specifications

Specification	Design objectives	CMOS design	CNTFET design
Slew Rate	≥ 4V/µs	4,609V/µs	9,76V/µs
$ICMR^+$	≥ 0,3 V	0,187 V	0,473 V
$ICMR^-$	≤ -0,3 V	-0,608 V	-0,844 V
GBW	≥ 8 MHz	9 MHz	8.84 MHz
Voltage Gain	≥ 40 dB	40 dB	96.45 dB
Phase Margin	≥ 60°	91°	90°

Table 2 - Transistors sizes for CMOS and CNTFET differential amplifier designs.

Transistor	CMOS design		CNTFET design	
	W	L	N	L
M1=M2	3000 nm	300nm	2	100nm
M3=M4	400nm	110nm	1	70nm
M5=M6	800nm	45nm	4	32nm

6. REFERENCES

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