DESIGN OF A 2.4GHZ CMOS LOW NOISE AMPLIFIER

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ABSTRACT

This paper presents the design of a low noise amplifier (LNA) operating at 2.4GHz, using a 0.18µm CMOS XFAB technology. Inductive source degeneration topology is used, because of its good trade-off between gain and noise. Two different LNA circuits were implemented, and based on the simulation results we have chosen a circuit which presents a gain of 8.2dB and a noise figure of 2.32dB, for a power consumption of 27 mW. All the design steps are presented: gain optimization, input and output impedance matching, insertion of cascode stage, stability and noise figure analysis. The layout of the final circuit is presented at the end of the paper.

1. INTRODUCTION

One of the main blocks a receiver system is the Low Noise Amplifier (LNA). Its main function is to provide enough gain to overcome the noise (noise here is understood as anything other than information relevant to the system) of the following stages (e.g. a mixer) [1]. On the other hand, the LNA should add as little noise as possible to minimize the impact on overall performance, since its noise figure is directly added to signal to noise ratio of the whole system [2]. Another challenge is to accommodate signals as large as possible without distortion, i.e., provide a good linearity, and to present a specific input impedance to guarantee a good performance of the band pass filter followed by the antenna and a maximum power transfer. Most transceivers operate with standard termination impedances, generally 50Ω [2]. An additional requirement is low power consumption, which is especially important for battery-powered communication systems [3].

This paper is organized as follows. Section II reviews the properties of inductive source degeneration topology used in this work. Section III presents the LNA design. Preliminary results and conclusions are discussed in Section IV.

2. TOPOLOGY

The low noise requirement leads us to the use of only one active device at the input of the LNA [4]. By analyzing MOSFET two-port noise parameters, the source impedance that yields minimum noise factor is inductive and generally unrelated to the conditions that maximize power transfer. Moreover, it's difficult to provide a good matching for 50Ω source impedance without degrading the noise performance, because the MOSFET input impedance is inherently capacitive [1]. The best compromise between input matching and noise figure is achieved by using inductive source degeneration shown in Fig.1, which allows to obtain a real input impedance without the use of a resistor.

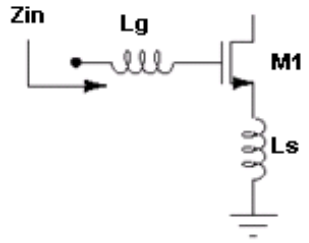

Fig.1 Inductive source degeneration topology

To simplify the analysis, consider a device model that includes only g_m and a gate-source capacitance, whose input impedance has the following form:

$$Z_{in} = \frac{1}{sC_{gs1}} + s(L_s + L_g) + \frac{g_m L_s}{C_{gs1}} \qquad (1)$$

Where C_{gs1} is the gate to source capacitance of M1, L_s is the degeneration inductor, L_g is the gate inductor and g_m is the transconductance. As can be seen from equation (1), the input impedance is composed of two parts, one real part which is independent of frequency and an imaginary part which is frequency dependent. The amplifier will be matched to 50Ω at the input, which leads us to two different equations:

$$\frac{1}{sC_{gs1}} + s(L_s + L_g) = 0 \qquad (2)$$

$$\frac{g_m L_s}{C_{gs1}} = 50\Omega \qquad (3)$$

Thus, the input impedance is the same of an RLC series circuit with the resistive term directly related to inductance L_s. But we can also note from the equations, that the input impedance is purely resistive only at resonant frequency [1].

3. LNA DESIGN

3.1. Gain optimization analysis

Our work starts by studying ne5rf transistor available in the XFAB XC018 technology. This transistor is made for RF applications. To analyze its ability to provide gain at high frequencies, the transistor is biased and its maximum available gain (G_{max}) is extracted from S-parameter simulations at various bias currents. Figure 2 shows the dependence of G_{max} on the bias current of a transistor with 16 fingers of L=0.5µm and W=20µm.

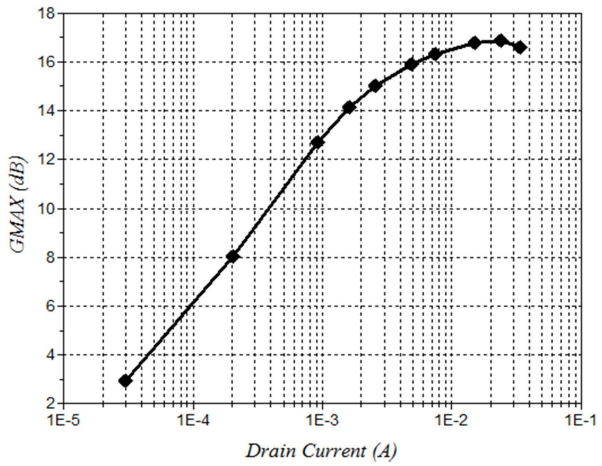

Fig. 2 - G_{max} of ne5rf, V_{DS} = 2V

For a bias current of 5mA the transistor can already provide a gain of 16dB, and the gain saturates for higher values of bias currents.

3.2. Choice of inductors

The technology we use provides only two values of inductance: 2nH and 3.8nH, limiting optimization freedom. Due to this limitation the choice of the inductances was made as follows:

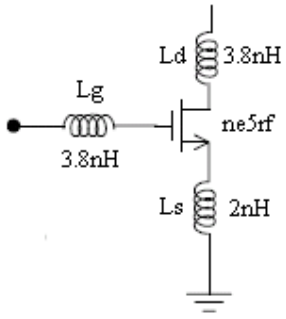

Fig.3 – Circuit with inductors of the technology.

Inductive degeneration should be as small as possible, because smaller L_s implies higher gain. L_g should be ideally large to improve circuit performance in terms of noise.

3.3. Input and output matching

A LNA should be matched at input and output to provide minimum reflection as possible, consequently a maximum power transfer. Here, S-parameters are fundamentals too, because we can easily analyze input and output impedance as S11 and S22 respectively, with the support of the Smith Chart.

The best way to match the input is manipulating values of C_{gs} and L_s from equation (3) (when you have degrees of freedom of inductance). In our case, the value of L_s has already been determined (2nH), which leads us to vary only C_{gs}. By analyzing simulation results, we concluded that the transistor had a very small C_{gs} even with the maximum value of W allowable (20µm) and the largest number of fingers (16), preventing the input matching. The solution was to insert an external capacitor (C_{gs2}) between gate and source, to increase the total gate-to-source capacitance.

The next step is to match the output. Analyzing S22, the way to match the output is with series and parallel capacitors. After matching the output, a small change occurs at the input, which is easily solved reducing the capacitance of C_{gs2}.

3.4. Stability

The LNA may become unstable due to the presence of feedback paths from the output to the input for certain combinations of source and load impedances. To test the stability of a circuit, we used the K and Δ parameters [2]. If K>1 and Δ<1, then the circuit is unconditionally stable, i.e., any combination of source and load passively realizable impedances will not result in oscillation. The difficulty in using K is that it needs to be calculated for a wide frequency range [2].

In this work, we observed in simulations that K remains greater than one and Δ smaller than one for the frequency range considered (1kHz to 100GHz). Another way to visualize stability is to look for oscillation conditions (Barkhausen criterion) at the frequency range considered. This method was also tested, and showed that indeed there is no condition for oscillations.

3.5. Cascode stage

Cascode stages are often used in this topology, due to enhanced reverse isolation (S12) and also to reduce effect of Cgd of the main transistor [1]. After the insertion of cascode stage, the reverse isolation indeed improved but the gain remained practically the same. The drawback in this case is the necessary increase in V_{DD}, to avoid the triode region of the main transistor.

3.6. Noise figure analysis

One of the main specifications of an LNA is its noise figure. It accounts for the degradation in the signal-to-noise ratio when the signal crosses the device, and corresponds to the noise factor expressed in db. The analysis of noise figure was fundamental in the choice of the circuit. The results are presented in the next section.

4. RESULTS AND DISCUSSIONS

The following table summarizes the performance in terms of S-parameters, noise figure (NF) and power consumption of the two circuits implemented. Figures 4 and 5 present the respective schematics.

	LNA without cascode (Fig. 4)	LNA with cascode (Fig 5)
S11	-17.18dB	-19.5dB
S12	-20.94dB	-52.9dB
S21	8.20dB	9.53dB
S22	-31.35dB	-41.60dB
NF	2.32dB	3.49dB
Power consumption	27.35mW	40.6mW

4.1. Circuit schematics

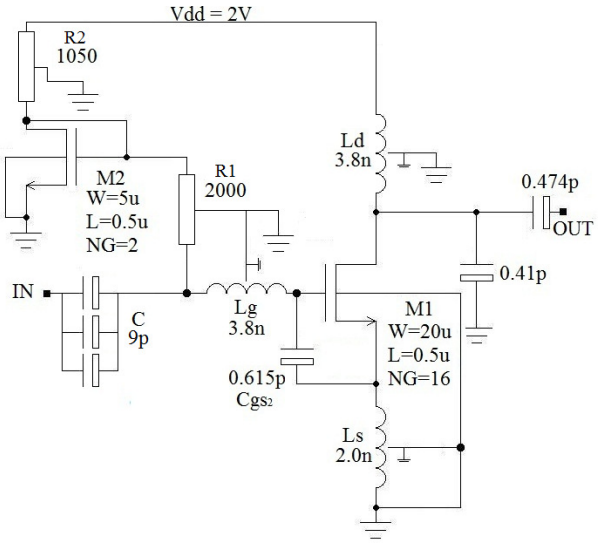

Fig.4 – LNA circuit.

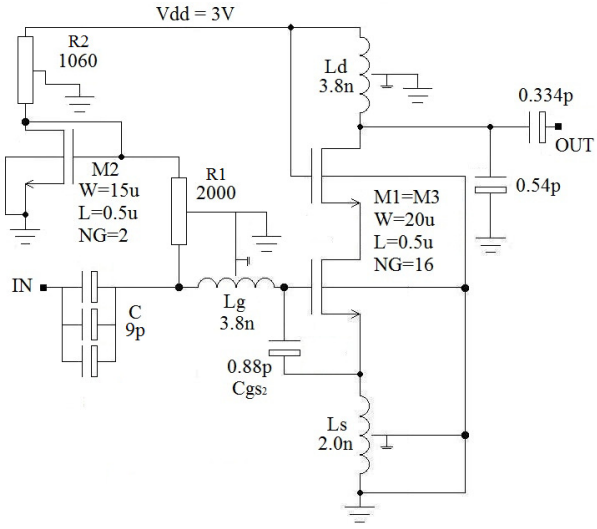

Fig.5 – Circuit of Fig.4 with a cascode stage.

4.2. Discussions

The initial idea was increase LNA gain with the insertion of cascode stage, since this work has no power consumption constraint. By analyzing the simulation results, we concluded that with the insertion of a cascode stage the noise figure is substantially impacted. So we opted to proceed on the layout of the solution without cascode (Fig. 4), because it presents a reasonable gain, a good noise figure (within our specifications) and lower power consumption. The final layout is presented in Fig. 6, and the die area is about 1mm^2.

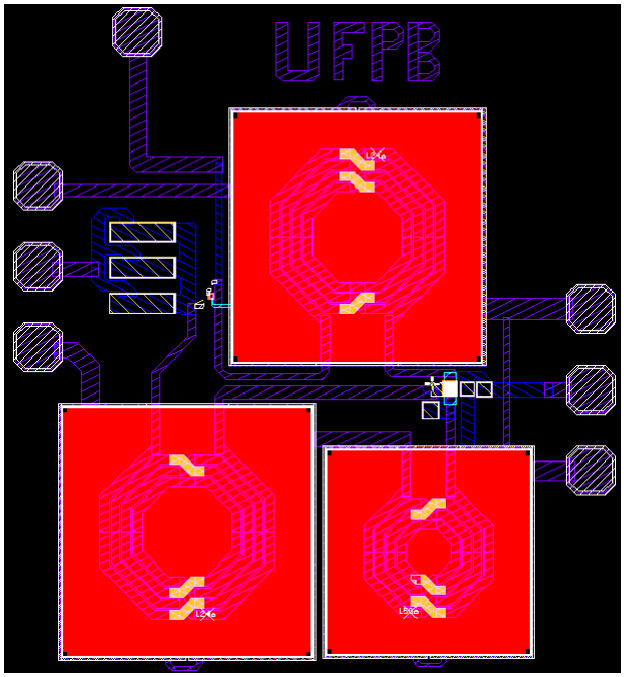

Fig.6 – LNA Layout. Input at the left, DC bias at the top, and output at the right.

5. REFERENCES

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