STUDY OF ANALOG PARAMETERS OF SUBMICRON GRADED-CHANNEL SOI MOSFET

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ABSTRACT

The study of the performance of graded-channel SOI transistors for analog applications is deeply related to the technology development on the microelectronic field. To overcome this challenge, it is necessary to acquire and to improve the knowledge of the parameters which characterize the device and to confirm if its performance remains better than uniformly doped transistors in advanced technologies. The present study brings a comparison between submicron standard (uniformly doped) SOI and graded-channel SOI nMOSFETs with different total channel length and L_{LD}/L ratio. The threshold voltage, subthreshold slope, maximum transconductance, output conductance and the intrinsic voltage gain were used as figure of merit for this analysis. First of all, some relevant results are presented from numerical two-dimensional simulations using Sentaurus device simulator and, after that, the tendencies of these results are experimentally verified.

1. INTRODUCTION

All the important advantages of using the Silicon- On-Insulator (SOI) transistors over bulk devices are already well known [1]. As many research groups have reported, devices that have a buried oxide layer, which characterizes the SOI technology, are faster because their junction capacitances are strongly reduced with respect to bulk devices [1].

Today, the compromise is not only to develop the SOI technology, but to create new structures that, associated to the benefits from SOI, can improve even more transistors performance.

The Graded-Channel (GC) SOI transistor is an interesting proposal of device, which has shown improvements for analog circuit applications [2]. GC devices have an asymmetrical doping profile in the channel region: the source side of the channel presents higher doping level and is responsible for the threshold voltage control; the remaining part of the channel, with length L_{LD}, is kept with natural wafer doping level, as shown in Figure 1.

The asymmetrical doping profile causes a reduction in the effective channel length (L_{eff}), since the lightly doped region works as an extension of the drain region under the gate. So, the effective channel length may be considered $L_{eff} \approx L\text{-}L_{LD}$, as a first approximation [3]. This doping reduction also allows a reduction of Parasitic Bipolar Effects, such as impact ionization [4], increasing breakdown voltage and reducing the output conductance. The benefits brought by the GC SOI transistors change according to the ratio L_{LD}/L [5].

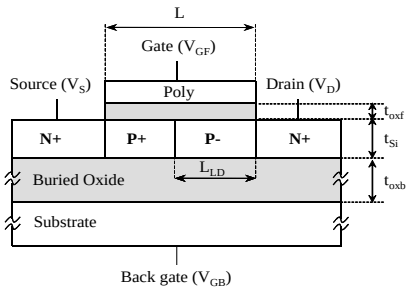

Figure 1 – Cross-section of a GC SOI nMOSFET.

According to Colinge [1], the intrinsic voltage gain (A_v) of a MOSFET can be expressed by the transconductance (g_m) divided by the output conductance (g_D):

$$Av = \frac{gm}{gd} \tag{1}$$

In this work basic parameters of GC and standard transistors are presented as a function of the total channel length and L_{LD}/L ratio, as well as the intrinsic voltage gain. Theoretical data from two-dimensional simulations and experimental measurements compose the results presented in this study.

2. SIMULATION

Two-dimensional numerical simulations were performed using Sentaurus Device Simulator (SDEVICE) from Synopsys [6]. For these simulations, an input file describes the structure to be simulated (materials, doping concentrations, etc.) and the analytical models to consider the desired effects. The chosen models will be presented in the following section.

To solve continuity and Poisson equations, SDEVICE uses the finite element method. As the simulator considers temperature effects, it was set 300K for the simulations.

The simulated transistors have the same characteristics of those fabricated at the Microelectronics Laboratory of Université Catholique de Louvain (UCL), Belgium, and available for measurements.

All the devices have the following dimensions, indicated in Figure 1: front gate thin oxide thickness (t_{oxf}) equals to 30nm, silicon film thickness (t_{Si}) equals to 80nm and buried oxide thickness (t_{oxb}) equals to 390nm. Moreover the doping concentrations at the source side (N_{AH}), lightly doped side (N_{AL}) and at the source/drain regions (N_D) are equal to $6x10^{16}cm^{-3}$, $1x10^{15}cm^{-3}$ and $5x10^{20}cm^{-3}$, respectively.

Transistors with channel length (L) of 2µm, 1µm and 0.75µm were simulated, considering L_{LD}/L ratios raging between 0 (that corresponds to the uniformly doped standard device) and 0.6. The transistors with channel length of 0.75µm were made with source and drain regions advancing 0.1µm inside channel region (Figure 2). This strategy has been used to better reproduce short-channel effects.

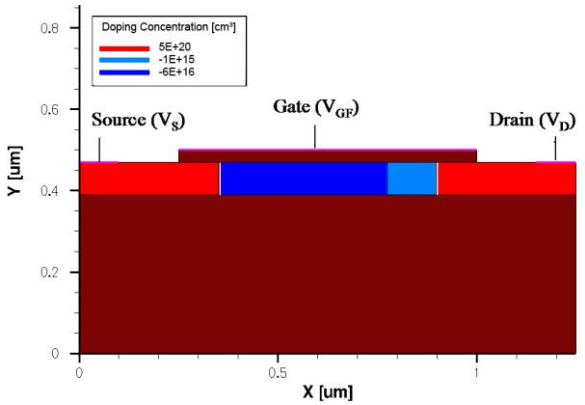

Figure 2 – Transistor structure illustration. L=0.75µm, L_{LD}/L = 0.3.

2.1. Models

In these simulations, it was used PhuMob model, which is a unified mobility model that describes the carriers' mobility, their temperature dependence and still comprises scattering and some impurities effects; Enormal model that is responsible for the mobility dependencies on the normal electric field and HighfieldSaturaion model, which is responsible for velocity saturation and driving force of the carriers in high electric fields; Avalanche (vanOverstraeten) model that considers the impact ionization effect.

The UniBo model was also included in Enormal model to render the transconductance curve more similar of that that was expected. This submodel was developed by University of Bologna to fit the simulated results in experimental data.

2.2. Parameters Extraction

Figure 3 shows drain current (I_{DS}) *versus* front gate voltage (V_{GF}) curves for standard SOI and GC SOI transistors simulated considering V_{DS}=50mV.

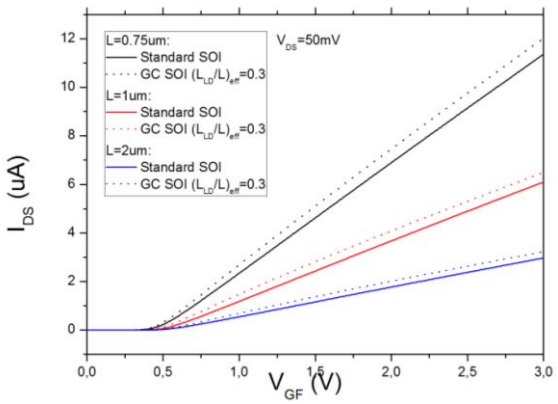

Figure 3 – I_{DS} vs. V_{GS} curves of GC and standard devices with different total channel lengths, biased at V_{DS} = 50mV.

The threshold voltage (Vt) has been extracted from I_{DS} vs. V_{GF} curves at low V_{DS} (50mV), using the second-derivative method [7] and the obtained results for the simulated devices are presented in Table 1. Also in this table the subthreshold slope and the maximum transconductance at low electric field (V_{DS}=50mV) have been presented.

Table 1 – Extracted parameters for the simulated devices

Device	Vt (V)	$gm_{máx}$ (µS)	S (mV/dec)
L=2µm - SOI	0.50	1.23	65.0
L=2µm - GC SOI L_{LD}/L=0.3	0.49	1.42	65.2
L=1µm - SOI	0.48	2.51	66.4
L=1µm - GC SOI L_{LD}/L=0.3	0.47	2.86	69.0
L=0.75µm - SOI	0.45	4.58	75.4
L=0.75µm - GC SOI L_{LD}/L=0.3	0.43	4.93	76.1

From the results shown in the table, it is possible to note a decrease of the threshold voltage in two situations: as the channel length decreases between devices of the same technology and as the L_{LD}/L ratio increases for the same channel length devices. In both cases, this Vt reduction is caused by the occurrence of short-channel effects, observed when either the total channel length or the effective channel length (L_{LD} increase) is reduced.

Although GC SOI transistors exhibit larger maximum transconductance values, they also show a worsening for the subthreshold slope than uniformly doped devices with the same channel length, as they present shorter L_{eff}.

3. EXPERIMENTAL MEASUREMENTS

The devices used in this study were fabricated according to the process described in reference [8]. All measured transistors present length and other geometrical parameters equal to the simulated ones, apart from the channel width (W), which is of 20 µm for the measured samples. The layout of the measured transistors is presented in Figure 4. The experimental current as a function of the applied voltage have been obtained with a Keithley 4200 Semiconductor Characterization System with medium integration time.

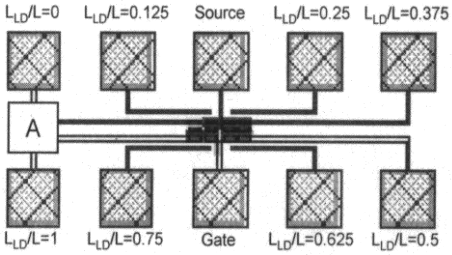

Figure 4 – Transistors' layout

The L_{LD}/L ratio indicated in Figure 4 corresponds to the designed mask ratio, which means that these values are not real, but the ratio which was intended before fabrication process. To calculate the effective ratio of

fabricated devices, noted as $(L_{LD}/L)_{eff}$, one can use expression (2) [4], which is valid in the beginning of the saturation region.

$$\left(\frac{L_{LD}}{L}\right)_{eff} = 1 - \frac{I_{DS}}{I_{DS,GC}} \quad (2)$$

Figure 5 shows experimental drain current *versus* front gate voltage curves for standard SOI and GC SOI transistors with V_{DS}=1V. This figure presents the experimental results for devices with $(L_{LD}/L)_{eff}$ ratio close to the simulated ones, shown in Figure 3 and Table 1 (L_{LD}/L=0.3).

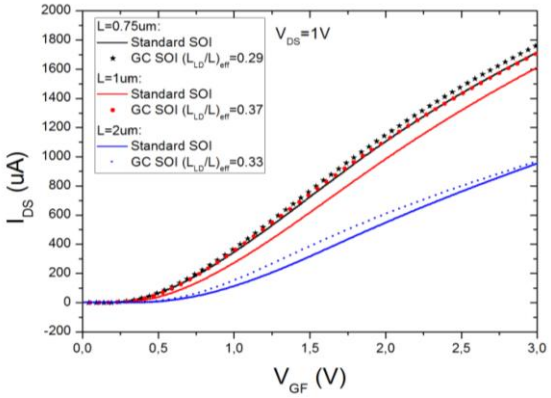

Figure 5 – I_{DS} vs. V_{GS} curves of GC and standard devices with different total channel lengths, biased at V_{DS} = 1V.

Figure 5 shows that drain current increases as the total channel length decreases. Also I_{DS} is larger for GC devices and increases as the L_{LD}/L increases, due to the effective channel reduction. This fact reveals that GC SOI has a better performance considering the current level.

Basic electrical parameters were also extracted from measured I_{DS} vs V_{GF} curves at V_{DS}=50mV and the results are presented in Table 2. For these experimental results, it is relevant to note that Table 2 shows the same trend for the threshold voltage, maximum transconductance and subthreshold slope values presented in Table 1.

Table 2 – Extracted parameters obtained for the experimental measured devices

Device	Vt (V)	$gm_{máx}$ (µS)	S (mV/dec)
L=2µm - SOI	0.39	0.276	65.4
L=2µm - GC SOI $(L_{LD}/L)_{eff}$=0.33	0.37	0.319	66.7
L=1µm - SOI	0.29	0.533	65.6
L=1µm - GC SOI $(L_{LD}/L)_{eff}$=0.37	0.25	0.614	68.9
L=0.75µm - SOI	0.23	0.589	69.6
L=0.75µm - GC SOI $(L_{LD}/L)_{eff}$=0.29	0.22	0.630	72.0

4. ANALOG PARAMETERS

After obtaining the results in the Tables 1 and 2, it is possible to go ahead to the first aspect that characterizes the analog characteristics of GC transistors.

As mentioned earlier, the intrinsic voltage gain is given by the ratio between g_m and g_D. Figures 6 and 7 present the transconductance and output conductance of the simulated devices, respectively. To extract the transconductance (g_m) and the output conductance (g_D) it was used the following bias point: 1V applied to the drain contact and $V_{GT}=V_{GF}$-Vt=200mV.

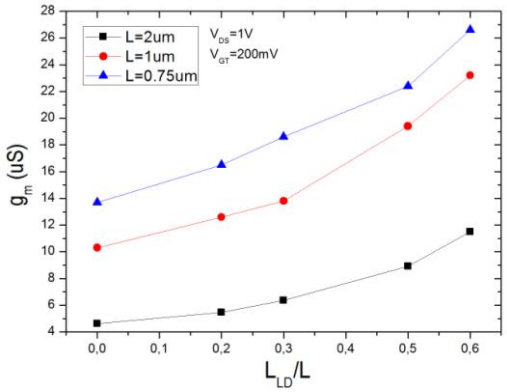

Figure 6 – g_m *versus* (L_{LD}/L) to simulated devices.

Figure 6 shows how g_m increases as the effective channel length decreases, which means that small channel lengths (caused by larger lightly doped region) characterize devices that have a better control of the drain current by the gate contact.

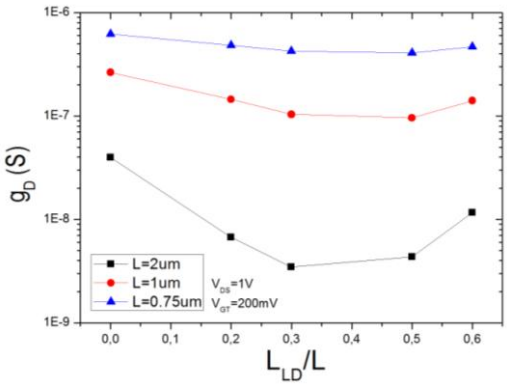

Figure 7 – g_D *versus* (L_{LD}/L) to simulated devices.

Figure 7 shows that the best values for output conductance belong to the longer devices, in other words, as longer the channel length smaller the output conductance. As the L_{LD}/L ratio increases, it is possible to note improvements at g_D response, once the lightly doped region reduces the potential on the effective channel region. The smaller potential drop in the highly doped channel region reduces the channel length modulation effect, which is responsible for the output conductance growth [9]. However, there is a point where the devices start suffering the short channel effect and the effective channel length become so small that the output conductance increases.

4.1. Intrinsic Voltage Gain

Applying Equation (1) for all the simulated and measured transistors studied in this work, the voltage gain

of the devices (Av) was extracted and is presented in Figure 8. In this figure, solid lines indicate the simulated transistors (also named as SIM) and the dotted lines indicate the measured ones (MEAS).

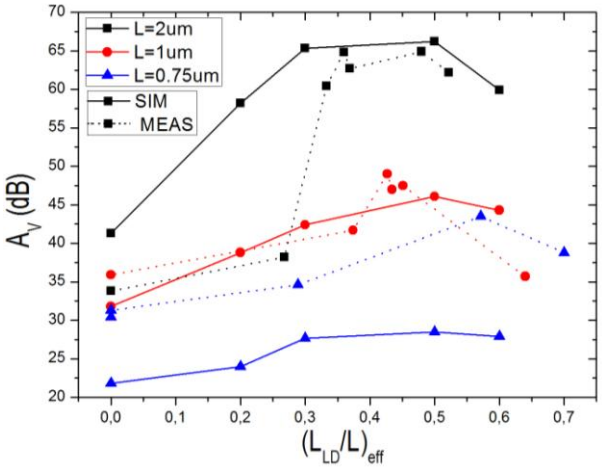

Figure 8 – Intrinsic voltage gain as a function of the ratio $(L_{LD}/L)_{eff}$ extracted for simulated and measured devices.

Although the tendency of the simulated and the measured devices is the same, Figure 8 indicates that it is necessary to make some adjustments in the simulated devices in order to make them more similar to the measured results. It is worthwhile mentioning that no optimization of model parameters has been made in the simulations, which is beyond the scope of this analysis and may affect the quantitative results but does not affect the qualitative analysis and trends.

The voltage gain follows the inverse of g_D curve, since the transconductance always increase with the L_{LD}/L increasing. As it is possible to verify, when the transistors become smaller, their transconductance increases and provide more drain current, but this scaling has also undesirable implications in the output conductance, as shown in Figure 7, causing the intrinsic voltage gain decrease as the channel length is reduced, as shown in Figure 8. This Av degradation is in GC SOI transistors, although it still presents larger gain than standard uniformly doped transistors with similar total channel length.

5. CONCLUSIONS

In this work a study of graded-channel SOI transistors has been presented, by means of simulated and experimental data. As expected, the use of GC devices promotes the transconductance increase and output conductance decrease.

These improvements can be verified for the entire range of channel lengths and they are the reason why the GC SOI has a better performance than uniformly doped transistors.

Larger voltage gain was obtained for GC devices, due to the increase of g_m but mainly due to the reduction of g_D. However, for large L_{LD}/L ratio, GC devices start suffering from short-channel effects and loose performance.

It is worthwhile noting that to optimize the use of GC devices, transistors with $(L_{LD}/L)_{eff}$ around 0.4 and 0.5 must be chosen, since they have shown the highest voltage gain results.

The intentions for future works are to keep studying, through simulations and measurements, graded-channel SOI MOSFET transistors and others technologies. Besides that, to start implementing analog circuits using these transistors, for example current mirrors and amplifiers.

6. REFERENCES

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Acknowledgments

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