COMPARATIVE ANALYSIS SYSTEM FOR RADIATION TOLERANCE IN SRAM MEMORY CELLS

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ABSTRACT

A SRAM memory system designed to analyze single event upsets (SEUs) is presented. It contains two different memory cell banks and also the peripheral circuits to perform the control of the read/write operation. Project, simulation results and layout of the integrated circuit were made to validate its functionality. CMOS technology was used. IC characterization and test with the aid of Labview programming facilitates the research of the memory cell tolerance to radiation-induced effects.

1. INTRODUCTION

Natural sources of radiation present in the space (e.g. Van Allen Belts, solar flares, solar wind and cosmic rays) are known since the first space experiments [1]. In fact, even at ground level we are subjected to radiation effects. Integrated circuits have their characteristics changed due to strikes with particles (e.g. protons, neutrons, heavy ions, etc.) and it's a great concern in harsh environments. In MOS technology, long term exposure can cause threshold variation (Vth), mobility degradation, and an increase of the leakage current. Collisions in sensitive regions of a microelectronic circuit can bring what it's called Single Event Effects (SEEs [2]) and may cause malfunctioning (analog and digital circuits) in a short time (few ns). As examples of transitory effect, we have Single Event Latchup (SEL) that may lead to device failure, whereas in memory circuits SEU [3] may cause loss of information.

Charge deposition and transport are consequence of ionization and are behind the SEEs. When a particle reaches the semiconductor material, electron-hole pairs are generated and reversed bias p/n junctions can collect these carries. The amount of charge deposited is related to the target material, type of particle and the incidence angle. MOS transistors in the cutoff region may turn on, disturbing the voltage at drain. In a SRAM cell, this transient voltage propagates through the circuit, leading to bit inversion if it has enough energy.

A robust design is achieved by using techniques such as system level hardening (triple modular redundancy (TMR) and error detection and correction (EDAC) [4]), circuit level hardening that relies with different memory cell topologies, and finally the use of other technologies such as SOI to reduce the amount of collected charge at the struck node (device-level hardening).

2. SRAM CELLS

The standard 6T cell (Fig. 1a) is commonly used in a memory array because of its better performance compared to others cells (e.g. 4T with resistive load and 4T loadless cell) [5]. It has a good compromise regarding packing density, stability (read and write margins) and power consumption. However, owing to SEU effect, this cell is not attractive in systems demanding high tolerance to radiation, such as in space applications.

Dual Interlocked Storage Cell (DICE) [6] is a circuit-level hardening approach to overcome SEU and its schematic is presented in Fig. 1b. This circuit isn't fully immune to SEU in case the nodes that store the same information (e.g. Q and Q´) are simultaneously hit by particles, causing bit flipping. Despite this inconvenience, the circuit is commonly used.

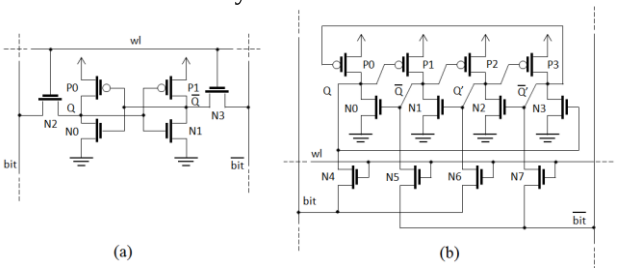

Figure 1. SRAM memory cells.

3. MEMORY SYSTEM

A typical memory presents a number of auxiliary circuits such as pre-charge, row/column decoder, sense amplifier, write driver, timing control and others in order to access its content [5]. These circuits are designed with extra driving capability to reduce the sensitivity to SEEs during tests in a particle accelerator. Otherwise, test data could be masked by their influence. Thus, memory cells are the most sensitive circuits in RAM system, as they are designed with small size for large integration.

To realize a comparative study, the storage elements were split into two banks, as it can be seen in Fig. 2. Each bank is organized in 32 rows and 32 columns (1024 bits). Pre-charge circuit is intended to speed up the bit processing time (read/write), by setting the bit lines to VDD-V*thn*. A better pre-charge voltage would be VDD/2, at cost of complexity and power increase due to the need of a voltage regulator or resistive dividers.

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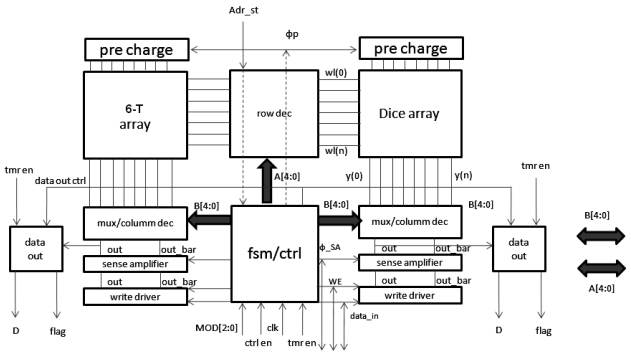

Figure 2. Block diagram of the system.

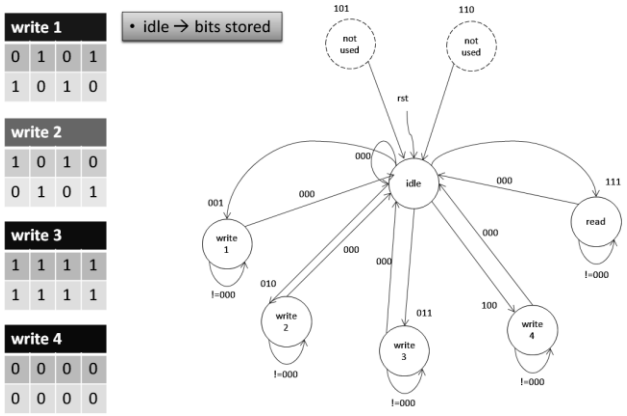

Figure 3. FSM states description.

Row decoder was designed to access both arrays at the same time. It has an address strobe input to guarantee that the address inputs are valid. Since a column decoder with a multiplexer is used to generate a single output, it's not necessary one sense amplifier for each column. Sensing circuits are needed to amplify the small differential voltage across bit lines during read operation. A writing driver circuit is used to overwrite the content of a cell memory and it's also a single unit for each bank.

The data-out circuit is composed by a latch and a flip-flop. Since they are memory elements, TMR is implemented to improve fault tolerance against SEU. Basically, this means that the information is stored in three equal banks and they are supposed to have the same information. A voter circuit will produce an output bit based on the fact that at least two circuits have the same information. Therefore, the probability of particles to cause SEU in the three sections at the same time is lower then if it was just one circuit. Flag signal indicates if one out of the three circuits has different information and then SEU can be detected at this block.

Timing control is done with a Finite State Machine (FSM) together with a synchronous binary counter. They were developed to sequentially write/read all the bits in the arrays. Counter generates both row and column addresses and the whole array is swept from bit #1 (first row and column) until bit #1024 (last row and column). Four write patterns are available to be passed into the arrays, therefore increasing the flexibility of SEU detection. Fig. 3 shows the state machine, in which the Idle state means that the information is only stored. Two unused states (101 and 110) point to Idle in case the FSM falls accidentally on them (e.g., upon power-up). MOD [2:0] bus controls the FSM, while TMR was also added as there are memory elements in this block. An option to externally generate all control signals is provided, with all addresses input to the chip.

Fig. 4 is an case example of signals for a 4x4 array (16 bits) at the Write #2 pattern. FMS flip-flops are sensitive to the fall edge of the clock, and after the MOD bus changes (rise edge through LabView), the process starts. Since a full bit operation is worked out in two clock pulses, the time spent to sweep the entire array is

$$T_{array} = 2T_{clk}\,NM \qquad (1)$$

where N and M are the number of rows and columns. Prior to the sweep cycle, the addresses are at 00, which activates the first row and the first column. But the decoders are designed to not allow this situation, as on Idle state there should be no activities. At the first clock pulse, column #1 is selected and the pre-charge is done (ϕp). At the second pulse, the write driver turns on (WE) and the release of row #1 is made through Adr_st signal (address strobe). The data_in signal imposes what is being passed onto the memory cells. Latch receives the data and passes onto the output flip-flop at the end of the cycle. Read cycle is done in a similar way, except for the activation of the sense amplifier (ϕ_SA) that occurs at the high transition of the second clock pulse. This is necessary to give enough time (low level) for the memory cell to shift the voltage level of the bit lines to ensure a correct operation of the sense amplifier.

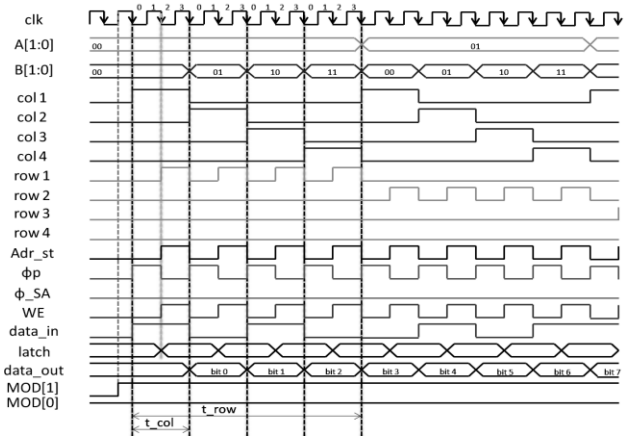

Figure 4. System waveforms.

The chip layout is presented in Fig. 5. Dimensions are: 1,234 µm x 874 µm (667 µm x 300 µm without pads). Column decoder and multiplexer were made only once since memory cell's layouts have the same width. Placement of the circuits was carefully taken, so as control signals have short paths. For example, the output of the counter is very close to the input of the decoders

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and the same applies to FMS outputs to the auxiliary circuits. Flip-flops belonging to FMS and data-out circuit are surrounded by substrate contacts to reduce charge collection. Since the voter circuit itself must be robust, transistors were laid out each one with substrate contacts around and a guard ring involving the whole circuit. Charge sharing due to a particle collision is then reduced with these techniques. A total of 36 pins are necessary. Power supply of the core is at 1.8 volts and the pad circuits are at 5 volts. Level shifters are used to perform the voltage conversion.

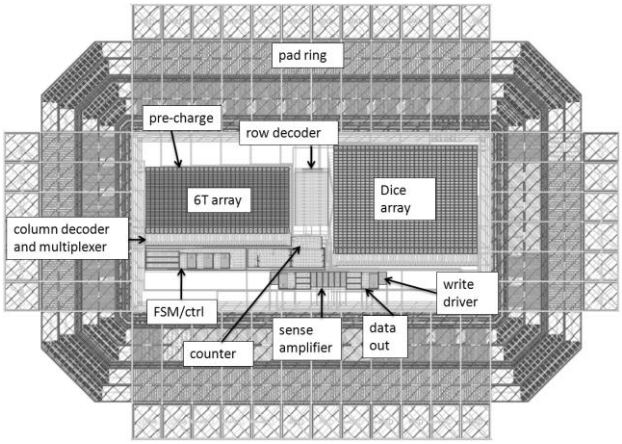

Figure 5. Chip layout.

4. TESTBENCH

Labview Virtual Instrumentation (VI) and data acquisition board make easier the characterization of the integrated circuit. The idea is to provide the system with the signals necessary for its operation and collect the data for analyzes. Although either an FPGA or a microcontroller could be used to control the system, the Labview graphical programming presents a friendly environment and intuitive to work with. Fig. 6 shows a panel for the VI. For example, once the Write 1 button is pushed, the signal generator provides the MOD bus pulse and the Address strobe signal. As the data from the arrays are generated, they are filled into the matrixes for later comparison. When read operation is being performed, it's expected to detect potential differences between the reference matrix and the exposed matrixes during testing under proton acceleration. A comparison function points out which bits have been flipped under radiation effect and a log file with errors is generated.

The PCB with the mounted IC is placed inside a special case to perform the radiation test. Since there is a limited number of cables that can be connected to this case, by generating the addresses inside the chip the count of wires is reduced. These connections, represents a reasonable capacitive load so that drivers are provided.

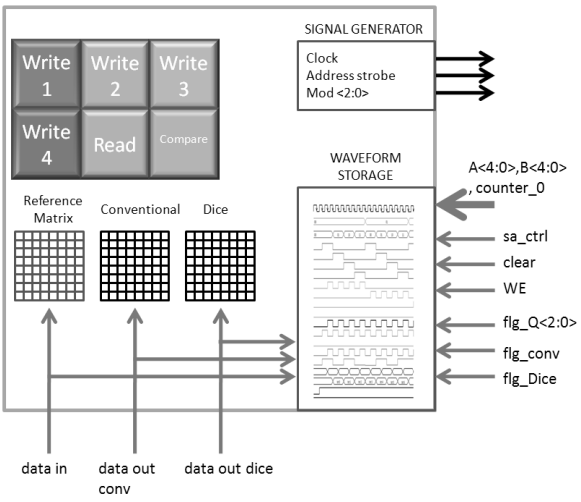

Figure 6. VI panel interface.

5. CONCLUSIONS

Electronic devices are subjected to the effects of energetic particles, and must be carefully qualified to assure its reliability. Analyzing the SEU demands an understanding not only for integrated circuits but also in tools that helps to gain insight in a system design and test. A SRAM memory system was proposed to investigate which memory cell features better tolerance to SEU.

6. REFERENCES

[1] R. Velazco, P. Fouillat and R Reis, "Radiation Effects on Embedded Systems", Springer, 2007.

[2] http://radhome.gsfc.nasa.gov/radhome/see.htm .

[3] P. E. Dodd and L. W. Massengill, "Basic Mechanisms and Modeling of Single Event Upset in Digital Microelectronics", IEEE Trans. Nucl. Sci., vol. 50, no. 3, June 2003.

[4] J. Abraham, E. Davidson and J. Patel, "Memory System Design for Tolerating Single Event Upsets", IEEE Trans. Nucl. Sci., vol. NS- 30, no 6, Dec. 1983, pp. 4339-4344.

[5] A. Palov, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies", Springer, 2008.

[6] T. Calin, M. Nicolaidis and R. Velazco, "Upset Hardened Memory Design for Submicron CMOS Technology" IEEE Trans. Nucl. Sci., vol. 43, no 6, Dec. 1996.

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