STUDY OF pMOS/nMOS SOI MuGFETs USING 2D NUMERICAL SIMULATIONS AND ELECTRICAL CHARACTERIZATION

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ABSTRACT

The focus of this paper is to present an analysis among double gate transistors for different channel lengths comparing the performance of pMOS and nMOS transistors. The main electrical parameters such as threshold voltage, subthreshold slope, transconductance and DIBL are presented. The results have been obtained to compare the efficiency and the behavior of these different transistors using 2D numerical simulations and electrical characterization. The results show that nMOS transistor with thin silicon film thickness have better performance and reduced short channel effects compared to the pMOS devices.

1. INTRODUCTION

Historically, it is observed in microelectronic evolution the coherence of facts in relation to Moore's Law, where integrated circuits become smaller than ever but with higher number of transistors and with better performance. The major goal is the performance improvement and higher speed in the devices and for that it has been changed mainly the geometry [1]. However, what has been watched through the years is that smaller devices are more difficult to be controlled and to be fabricated. As a result, unexpected behavior and characteristics not very attractive that are called short channel effects (SCEs) appear in the structures.

Among the short channel effects, DIBL (Drain Induced Barrier Lowering) is one of the most important effects and it shows the influence of the drain bias on the threshold voltage [2]. To avoid short channel effects new technologies have emerged such as the Silicon on Insulator technology (SOI MOSFET) that replaces the conventional wafers to the SOI wafers, improving the control of the charges in the channel region [1].

In a second moment, the evolution to multiple gates devices describes the influence of the gate bias in the channel control and in the device performance. Short channel effects are reduced when more than one gate are built around the channel [3].

Following the idea about gate region control, the UTB technology (ultra-thin body) has been reported as another possibility to avoid short channel effects and to improve the current level since the silicon film thickness is very thin, making the charge control improved at these devices [1].

Using 2D numerical simulations, the goal of this paper is to obtain a comparative study of the main electrical parameters in pMOS and nMOS MuGFET transistors. The results are confronted with the experimental measurements achieved from triple gate SOI transistors.

2. NUMERICAL SIMULATIONS

The numerical simulator used in this work is ATLAS from Silvaco [4]. This simulator uses mathematical models based on the physical equations that allow the extraction of different parameters and polarization conditions. It was considered models of mobility, lateral electrical field dependence, bandgap narrowing and recombination time based on carrier lifetime.

The features adopted in the simulations are presented in table 1 and they are based on [5]. However, the simulations consider a two-dimensional structure, disregarding the effects of a channel width variation. The impact of different channel lengths and silicon film thicknesses are analyzed in both type of transistors: nMOS and pMOS.

Table 1. Simulated set of parameters.

Parameter	***Values***
Channel length (L)	*30 ~ 410 nm*
Silicon film thickness (t_{Si})	*30, 60 nm*
Front oxide film thickness (t_{oxf})	*2 nm*
Buried oxide film thickness (t_{oxb})	*150 nm*
Channel Doping Concentration (N_a)	*$1x10^{15}$ cm^{-3}*
Source/Drain Doping Concentration (N_d / N_a)	*$1x10^{20}$ cm^{-3}*
Lightly Doped Drain (LDD) Concentration (N_{d_LDD}/N_{a_LDD})	*$1x10^{19}$ cm^{-3}*

The device structure used in the simulations is represented by the cross-section of figure 1. The same structure was simulated for pMOS and nMOS transistors changing only the type of material for each situation. In the case of pMOS, the doping concentration of the whole structure is formed by P-type material since the channel is naturally doped, according to [5]. Consequently the pMOS devices assume a P+/ P / P+ configuration while the nMOS transistors present the N+/ P / N+ well known structure.

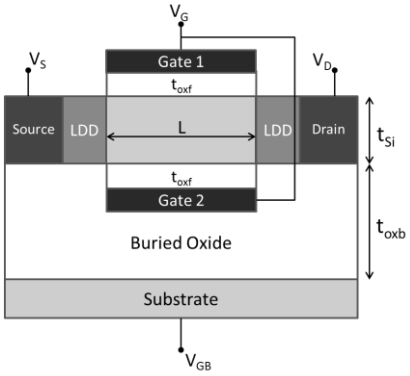

Figure 1. Cross-section of a double gate transistor.

3. SIMULATED RESULTS

The focus of this study is the difference between nMOS and pMOS transistors in terms of the main electrical parameters. The results obtained in the simulations are presented in the following items.

3.1. Threshold Voltage – V_{TH}

The values of threshold voltage were obtained from the maximum point of the second derivative of I_{DS} x V_{GS} curves. The work function adopted in the simulations is related to titanium nitride used as a metal gate of the process presented in [5]. For all situations, the values of V_{TH} are around 0.44 V, decreasing less than 10% with the channel length roll off. The thinner silicon film contributes to the stability of the values due to the better electrostatic control of the charges in the channel region.

3.2. Transconductance – gm

This parameter was extracted from the derivate of the I_{DS} x V_{GS} curve as suggested in theory. Transconductance curve allows making analyses in respect of the gate control on the channel region.

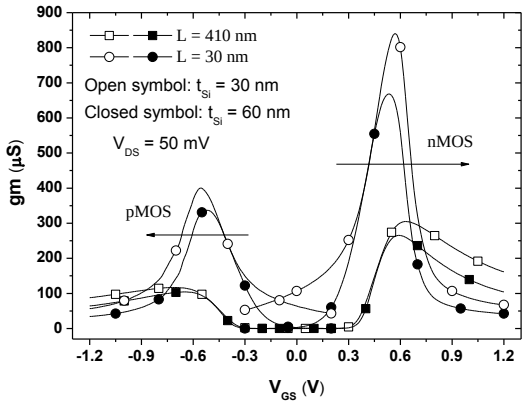

Figure 2. Transconductance as a function of gate bias for a short and a long channel lengths and t_{Si} of 30 and 60 nm.

The nMOS transistor presents higher gm values than the pMOS as presented by figure 2, which means that the higher mobility of the electrons directly affects the charges control since the dimensions are the same for both transistors.

The influence from the silicon film thickness increases the gm level due to the better current conduction when t_{Si} is smaller. The maximum transconductance as a function of channel lengths (figure 3) shows the improvement in the values for shorter devices as expected. The slight decrease occurred for the 30 nm nMOS devices can be associated to the influence of parasitic series resistance that becomes significant in those dimensions.

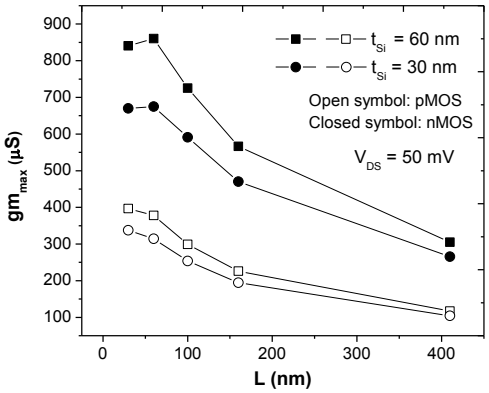

Figure 3. Maximum transconductance as a function of channel length for t_{Si} of 30 nm and 60 nm.

3.3. Subthreshold Slope – S

Subthreshold slope (also called slope or swing) was extracted from the inverse of the derivate of I_{DS} x V_{GS} curves in the subthreshold regime, considering a semi-logarithmic plot.

The subthreshold slope is defined as the efficiency of the transistor as a current switch. It is desirable small values of S that imply in faster transistors. The values of subthreshold slope are shown in table 2. The gates coupling is the responsible for the behavior improvement observed when a thin silicon film is used. The difference obtained is about five times smaller for the thin 30 nm-long devices. The channel length effect presents a higher influence in the subthreshold slope, increasing its values for the shorter lengths. The difference between pMOS and nMOS transistors occurs due to the influence of different carrier mobility.

Table 2. Subthreshold slope for different channel lengths and silicon film thicknesses.

L (nm)	pMOS		nMOS	
	t_{Si} = 30 nm	t_{Si} = 60 nm	t_{Si} = 30 nm	t_{Si} = 60 nm
30	168	893	161	858
60	75	167	74	158
100	64	86	63	83

3.4. Drain Induced Barrier Lowering – DIBL

This parameter shows the change in the threshold voltage value when the drain bias increases. This variation becomes worst for shorter devices and it is

calculated by the equation 1 [2], considering two different drain biases: 50 mV and 1.2 V. The threshold voltage values were extracted by the current level method.

$$DIBL(mV/V) = \frac{V_{TH1(VD1)} - V_{TH2(VD2)}}{V_{D2} - V_{D1}} \quad (1)$$

It is observed in figure 4 that for larger values of channel length and thinner silicon film no significant V_{TH} variation is obtained. For channel lengths below 70 nm the DIBL effect is highly pronounced particularly in t_{Si} = 60 nm, where the penetration of the field lines from the drain is higher compared to the smaller t_{Si} due to lower coupling of the gates, causing the threshold voltage variation.

The comparison between pMOS and nMOS can be better analyzed with the absolute variation and considering the smallest channel length for t_{Si} = 60 nm. At this condition, pMOS device presents almost 0.5 V/V of increase compared to the nMOS value. When a thin silicon film is considered, this difference is reduced to 40 mV/V, confirming the high influence of the horizontal field effect in the channel region for thicker silicon films. The percentage of DIBL variation along the channel is 51% for pMOS and 46% for nMOS with 60 nm of t_{Si}. The values reduce to 19% and 17%, respectively, for the thinner silicon film devices.

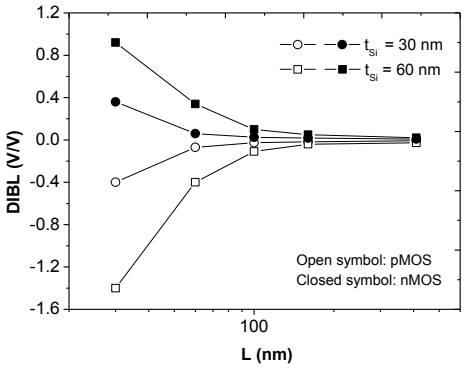

Figure 4. DIBL as a function of different channel lengths and silicon film thicknesses.

4. EXPERIMENTAL RESULTS

The electrical characterization was done using the HP 4156C equipment. The devices were fabricated at Imec (Interuniversity Microelectronics Center) in Belgium and they are triple-gate non-planar transistors.

The devices measured present five fins (N_{fins} = 5) and their main characteristics are presented in table 1, except for the channel lengths that varied from 60 nm to 910 nm. The major number of fins in parallel allows the increase of the transistor current level. This feature was not considered in simulations. The total width (W_{eff}) of non-planar transistors is given by $2H_{fin} + W_{Fin}$. The figure 5 represents the triple gate transistors with respective geometrical definitions.

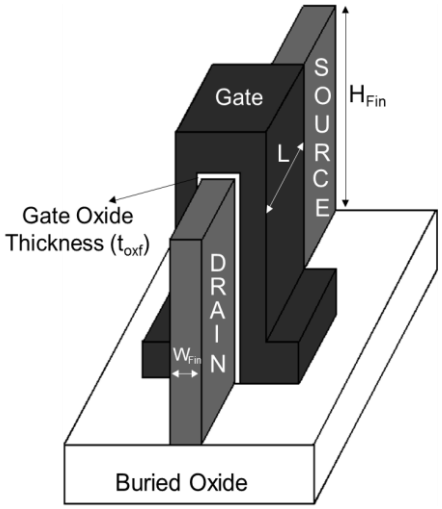

Figure 5. Schematic design of the triple gate device.

The transistors were measured by polarizing the drain with low (50 mV) and high potential (1.2 V). The gate voltage was varied from 0 to 1.2 V. In the case of triple gate devices, the third gate provides an improvement in the behavior of the device and therefore it is not possible to establish a direct comparison between the simulations and the measured devices. So, it is out of the scope of this paper to compare the results directly because more elaborate adjustments and 3D simulations would be necessary. However, the tendency in the results can be compared in order to estimate the reliability of the simulations. In this work the silicon film thickness is equivalent to the height of the fin (H_{Fin}) for the 60 nm condition that is the same for all measured devices. However it is common to associate the fin width (W_{Fin}) to the t_{Si} parameter since it is the distance between the gates [3]. Therefore, the variation in the fin width presents similar effects to those observed with the decrease of t_{Si}. Consequently, as there are two different fin widths in the set of measured devices it is possible to confront the results with the simulation ones.

4.1. Transconductance – gm

In figure 6, the maximum transconductance values do not follow the same trend obtained in numerical simulations. This is because the measured transistors are triple gate and the mobility between the sides and the top of the fin are not equal due to different crystallographic orientations. As a result, there is a competition of the type of the material and also the fin width influence that defines the current level and the transconductance behavior. Experimentally, pMOS devices present higher values of gm_{max}, considering the shorter structures, due to the high hole mobility on the sidewalls of the fin where the crystallography orientation is (110). The electron mobility is better in (100) orientation presented only on the top of the fin. The difference between nMOS and pMOS is around 15% for wider transistors and 7% for the narrower ones.

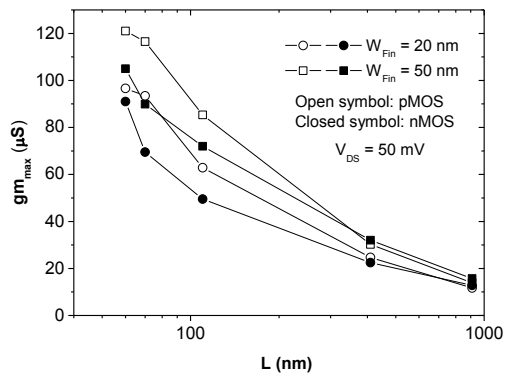

Figure 6. Maximum gm as a function of channel length.

4.2. Subthreshold Slope – S

The values of subthreshold slope can be observed in figure 7 where the influence from the different fin width is comparable to the silicon film thicknesses. Narrower fins improve the device behavior due to the better electrostatic coupling as well as the thin silicon films. The values of subthreshold slope are smaller for nMOS devices due to the different carrier mobility compared to pMOS devices, considering the exponential subthreshold regime. The difference obtained between pMOS and nMOS is approximately two times higher for the first case.

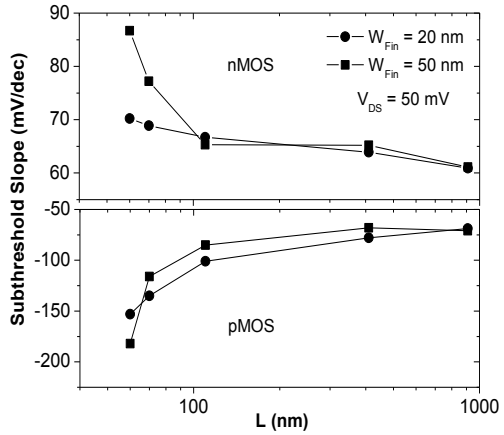

Figure 7. Experimental subthreshold slope as a function of channel length.

4.3. Drain Induced Barrier Lowering (DIBL)

The DIBL values are presented in figure 8 and the behavior is similar to that obtained in the simulations, presenting differences in the absolute values related to the set of approaches and the three-dimensional properties of the real devices. Decreasing the channel lengths, DIBL rises due to a higher interaction of the drain electrical field in the charges from the channel region. It is also observed that the largest variation of DIBL for short channel transistors occur for pMOS devices, mainly for the thicker silicon film condition where there is a percentage of 52% of increase in relation to nMOS. A possible reason to explain that behavior can be related to the different dopant diffusion that changes the charge profile in the channel region.

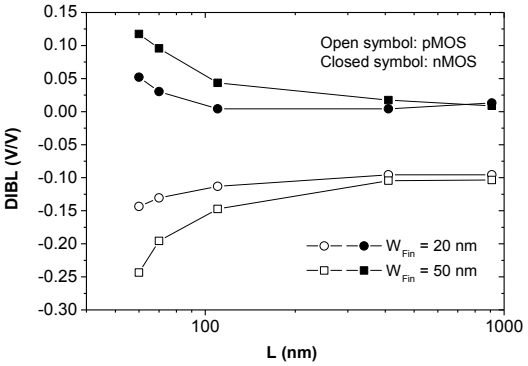

Figure 8. DIBL as a function of channel length for different silicon film thicknesses.

5. CONCLUSION

The paper analyses the main electrical parameters such as the threshold voltage, transconductance, subthreshold slope and DIBL. The study was done based on the comparison between pMOS and nMOS devices, varying the silicon film thickness for different channel lengths. It was observed that pMOS devices are more susceptible to the short channel effects, presenting higher values of DIBL and S which were obtained in both simulated and experimental results probably due to the different dopant diffusion. However, the maximum transconductance from the real devices showed to be better (higher) in pMOS ones due to the higher hole mobility on the sidewalls of the fin that was not considered in the 2D simulations. Devices using thin silicon film thickness were very efficient in the whole set of the studied parameters, improving the device behavior in terms of short channel effects and current level due to the better electrostatic coupling in the channel region. The same tendency is achieved when the fin width was varied in the experimental measurements. Comparing the experimental data to the simulated ones it was observed that there is the same tendency among them. The discrepancies that inevitably appeared derive from the fact that the real devices are triple gate non-planar transistors and the simulations were not fitted to work as the real devices. Consequently, the different carrier mobility on the top and on the sides of the fin and also the fin width influence contribute to the differences obtained.

6. REFERENCES

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