A Novel Method of Fabricating 3D Microelectronic Circuits Using Metal Wet Deposition over Oxidized Silicon

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ABSTRACT

The fabrication of microelectronic circuits aiming for 3D packaging using catalyst layer assisted metal wet deposition over oxidized silicon substrates is presented. This procedure showed excellent size resolution with improved edge definition and good adhesion to the substrate. The size and edge definition of the elements were measured using an optical microscope. The film adhesion was evaluated using adhesive tape test and wire-bonding pull-test. The wire pull-test of gold and aluminum wires resulted in a mean value of 3.5gf and 4.25gf, respectively. Two dies have been stacked together using non-conductive epoxy, with an alignment shift of ~2mm. The sample was packed into a standard ceramic capsule and the contact pads were wire-bonded for electrical measurements.

1. INTRODUCTION

Semiconductor materials are a key factor for many areas of advanced technology products such as electronic components, integrated circuits, optical devices, sensors and others. The construction of the devices and circuits depend on many factors related to the quality of the environment, purity of materials, etc. Metallization processes are a critical step in device and packaging fabrication and seriously affect the performance of the component [1, 2]. Electroless Nickel Phosphorous (Ni-P) deposition is a well known technique and has been used for selective deposition of metallic films and, in many cases, is an attractive alternative for metallization of back-end processes because it is a quick, low cost and low temperature process [3].

Furthermore, the continuous growth of the demand on electronic products, mainly portable ones, has driven the need for new packaging technologies that enable miniaturization and high integration [4]. In the context of System in Package (SiP) 3D packaging technology, this work used a single functional module composed by the vertical stacking of two or more chips which has applications in random access memories, MP3 players, video-audio gadgets, portable game consoles and digital cameras. This enables low cost high, silicon integration and area efficiency when compared to mounting them separately in a traditional way [4].

This paper describes a novel method of fabricating 3D microelectronic circuits employing metal wet deposition over oxidized silicon substrates. The interconnections die-to-die and die-to package were made by wire-bonding, the most popular method in chip stacking because of its low-cost and flexibility [4]. This stacking technology has been used by a number of companies, including Hitachi, Sharp, Amkor, Intel, and Hynix [4, 5]. The samples were analyzed in order to evaluate metal adherence, interconnect electrical performance and the feasibility of the 3D packaging structure developed.

2. EXPERIMENTAL PROCEDURE

2.1. Contact pads fabrication procedure

The substrates used in this study were single-side polished <100> orientated p-type silicon (Si) wafers (Boron doped with a resistivity of 1 – 10Ω.cm) with two inches diameter. Figure 1 shows the sequence of fabrication. Initially, the wafers were cleaned to remove all contaminants (organic and inorganic) from their surface. They were processed through a standard RCA clean composed by an SC1 step (1:1:5 NH_4OH:H_2O_2:H_2O @ 65ºC for 10min) followed by an SC2 step (1:1:5 HCl: H_2O_2:H_2O @ 25ºC for 10min) [6, 7]. A silicon dioxide (SiO_2) film of 0.8µm was thermally grown by wet oxidation in a horizontal hot-wall furnace at 1000ºC (Fig. 1A). Before catalyzation, the surface was activated by O_2 plasma (Fig. 1B) using a plasma etcher (Applied Materials) with the following etching parameters: O_2 flow of 20sccm, pressure of 50mTor, power of 900W, and duration of 10min. The deposition of the seed layer onto the silicon dioxide surface was performed by immersion in an aqueous tin(II) chloride solution (1g/l containing 4ml/l HCl) followed by activation in a palladium chloride solution (0.25g/l using 2.5ml/l HCl) [8]. The tin ions (Sn^{2+}) absorbed on the surface reduce the palladium ions

(Pd^{2+}). The colloidal palladium metal atoms form clusters and constitute the seed layer, which catalyzes the electroless nickel deposition [9, 10]. The subsequent step is to immerse the sample in a customized autocatalytic solution of Electroless Ni-P (Fig. 1C) similar to that reported by Dubin *et. al.* [11, 12], as described in Table I. The bath contains nickel chloride as a nickel ion source, sodium hypophosphite as a reducing agent, sodium acetate and ammonium chloride as complexing and buffer agents and lead(II) nitrate for stabilization. Sodium hydroxide (5N) is added to this bath for pH control. The deposition was performed under continuous stirring at a temperature of 60ºC, obtaining a film thickness of approximately 0.5µm. The main reactions induce by this bath are described in references [6, 13]. Deionized water with resistivity of 18MΩ.cm was used in all stage of the experiment.

Table I - Compounds and concentrations used on the Electroless Ni-P solution.

Compound	Concentration (g/l)
$NiCl_2.6H_2O$	15
$NaH_2PO_2.H_2O$	30
$CH_3C_2OONa.3H_2O$	10
NH_4Cl	50
$Pb(NO_3)_2$	4 ppm

Standard photolithography was used to define the 200 x 200 µm pads as shown in Figure 1D. The exposed Ni-P regions are thickened selectively with gold (Fig. 1E) using a commercial electrolyte solution (Auruna 553 UMICORE). The 1µm gold layer is used as a hard mask for the removal of the Ni-P by etching with an acid solution composed by 1:4.5 HNO_3:H_3PO_4 @ 60ºC for 30s as shown in Figure 1F.

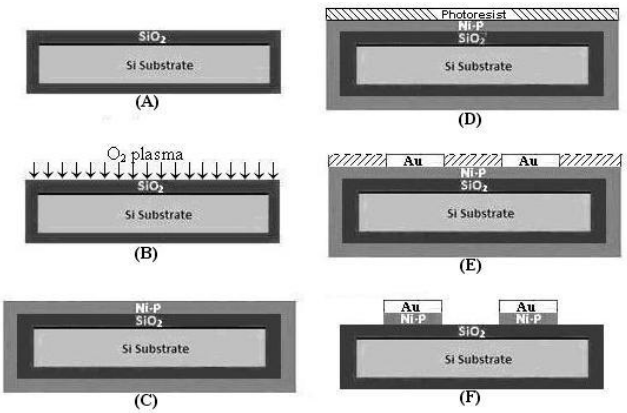


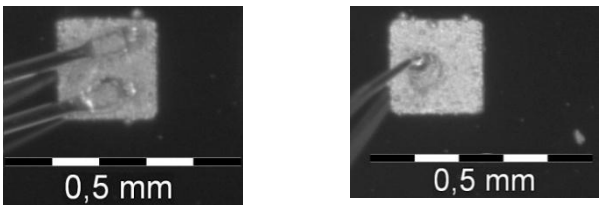
Figure 1 – Contact pads fabrication steps: (A) Substrate thermal oxidation; (B) Oxygen plasma activation; (C) Electroless Ni-P deposition; (D) Photoresist Deposition; (E) Selective electrolyte Au deposition; (F) Removal of exposed Ni-P.

2.2 Packaging procedure

The substrates were cut using a diamond saw, into 4mm x 4mm dies containing four sets of eight contact pads each.

One die was attached into a ceramic dual in line package (DIP) capsule, and a second die was then attached over the first one avoiding resin bleed over the contact pads of the bottom die. The adhesive layer used was a non-conductive epoxy (NCE) [14].

The interconnection of the stacked dies was achieved by wire-bonding. The aluminum (99%Al + 1%Si - diameter of 32µm) wiring was made using a compression machine (Sola Basic, EMB 1100 model) with a wedge-wedge connection as shown on Figure 2A. For the gold (99.99%Au - diameter of 17µm) wiring it was used an ultrasonic machine (TPT, HB16 model), obtaining a ball-wedge connection as showed on Figure 2B. The schematic drawing and an image of the final assembly of the stacked die package are shown in Figure 3A and 3B, respectively.



(A) (B)

Figure 2 – Images of the wire-bonding used: (A) Wedge connection for Al bonding; (B) Au ball connection.

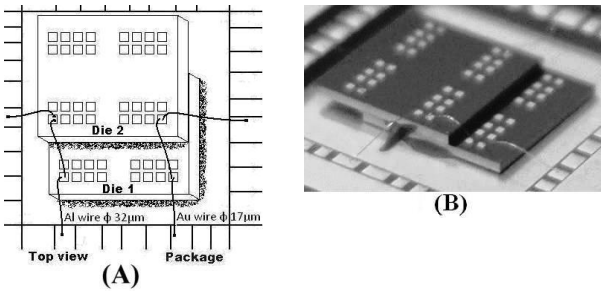


Figure 3 – (A) Schematic drawing and (B) image for the final assembly of the stacked dies.

3. RESULTS AND DISCUSSION

The oxygen plasma pre-treatment was performed in order to improve the adhesion of the Ni-P film to the silicon dioxide. The analysis by Fourier Transform Infra-Red (FTIR) spectroscopy, as shown in Figures 4A and 4B, indicates that the plasma treatment resulted in an absorbance increase of the SiO(r)"rocking" atom vibration, SiO_2(s) "stretching" atom vibration and Si-N-O groups. This change in the silicon dioxide surface most likely promoted the adhesion of the metallic film.

The metal adhesion was evaluated using Tape Test procedure, according to ASTM D3359 [15], resulting in

no removal of the gold structures from the substrate surface.

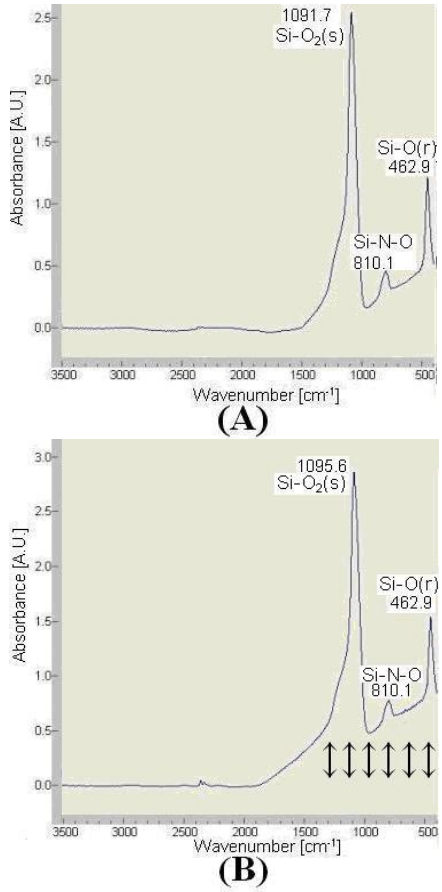


Figure 4 – FTIR spectroscopy measurements, showing the change in the absorbance, for the samples (A) before and (B) after oxygen plasma activation.

The connecting wires were submitted to the MIL-STD-883, 2011.7 destructive method [16], in order to measure bond strength (Fig. 5). The measurements were made by using a pull tester (HMP, 2350 NDL model) and the mean values for the gold and aluminum wires were 3.5gf and 4.25gf, respectively. These values easily exceed the minimum bond strength, approximately 2.0gf and 2.5gf respectively, provided by the above-cited method [16].

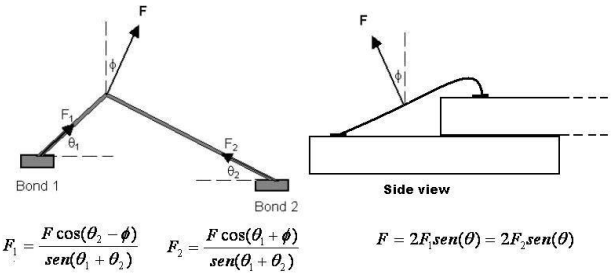


Figure 5 – Schematic drawing of the pull-test technique.

The electrical resistance was calculated from the I-V curves of the different elements (Fig. 6). The mean sheet resistance value for the contact pad (Au/Ni-P) is 0.862Ω, and wire resistances mean value for the gold and aluminum wires are 1.284Ω 1.415Ω, respectively.

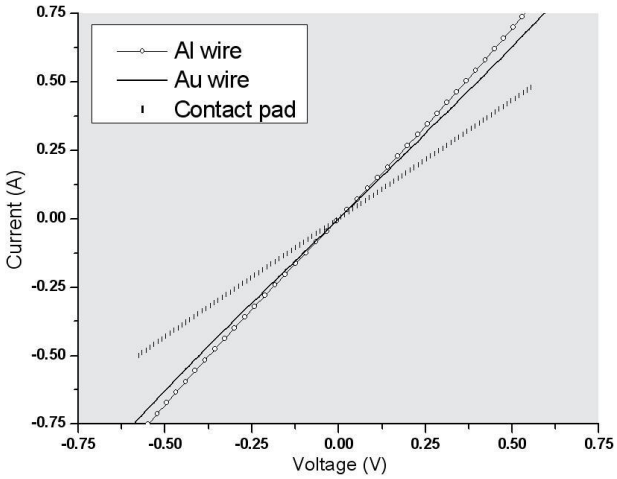


Figure 6 – I-V characteristics of the circuit elements.

4. CONCLUSIONS

We developed a method for the pre-treatment of the SiO_2 surface with O_2 plasma that enabled high adherence and good quality metal wet deposition onto oxidized silicon substrates. This novel method was successfully used for the fabrication of stacked dies 3D packaging.

The plasma treatment of the substrate surface leaded to the chemical bath deposition of metallic films (Ni-P and Au) with good adherence, uniformity and fine electrical characteristics. The fabricated structures also presented good edge definition, showing that our method is a low cost alternative to sputtering deposition, since it is necessary to obtain a base pressure value of ~ 10^{-6} mbar. The cost of high-vacuum sputtering equipment is known to be considerably higher than that used in our process (plasma pre-treatment followed by wet deposition).

The low resistance values of the contact pads and connecting wires, ranging in the interval from 0.86Ω to 1.41Ω, indicate that the wet chemical bath deposition method used in this study can be compatible with 3D packaging. This technique may results in an alternative solution for metallic thin films obtained by physical deposition methods due to its advantages, such as repeatability and low cost.

5. ACKNOWLEDGEMENTS

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