STUDY OF LOW TEMPERATURE INFLUENCE ON THE OPERATION OF CURRENT MIRRORS USING GRADED-CHANNEL SOI MOSFET

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ABSTRACT

This work presents a study of the use of a transistor with a different configuration in the channel region, named Graded-Channel (GC), for analog application in current mirror circuits with different architectures: Common-source, Cascode and Wilson. A comparison will be done between current mirrors implemented with standard (uniformly doped) SOI and GC SOI nMOSFETs by using simulation and experimental data to analyze mirroring precision and output resistance as function of temperature.

1. INTRODUCTION

The use of Silicon-On-Insulator (SOI) transistors has brought some improvements to the electronic circuits. The reason for the adoption of this technology to replace bulk one is related to the significant reduction of the junction capacitances due to the presence of a buried oxide layer, which isolates the active area of the transistor from the rest of the substrate, as well as the reduced short-channel effects [1].

The Graded-Channel device has as its differential characteristic an asymmetrical doping profile in the channel region, higher doping level at the source side than at the drain side [2]. The lightly doped region in the channel keeps the natural wafer doping profile level and its length is named L_{LD}, as shown in Figure 1, whereas the highly doped region is responsible for the threshold voltage control. The impact of having the total channel length divided as described results in the reduction of the effective channel length, L_{eff}, which can be approximated to $L_{eff} \approx L\text{-}L_{LD}$ due to the fact that the lightly doped region works as an extension of the drain, under the gate [3].

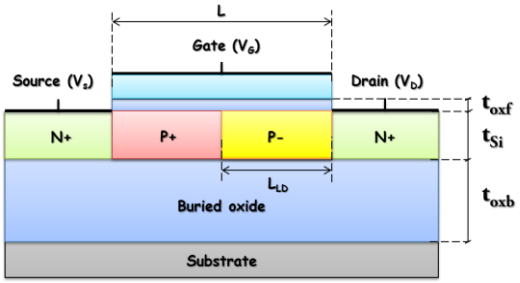


Figure 1 – Cross-section of a GC SOI nMOSFET.

This reduction of the effective channel length brings as advantages larger values for the drain current and, as consequence, higher transconductance (g_m), once they are inversely proportional to L_{eff}. Futhermore, the lightly doped region decreases the electric field at channel-to-drain junction and it provides smaller Parasitic Bipolar Effects, such as impact ionization [2], leading to higher breakdown voltage and reduced output conductance (g_D) [4]. Moreover, once the intrinsic voltage gain (A_V) and the unity-current-gain frequency (f_T) of a MOSFET is determined, respectively, by the expressions $A_V=g_m/g_D$ [1] and $f_T=g_m/(2*\pi*C_L)$, being C_L the load capacitance [5], GC SOI devices also present better results for these analog parameters [4].

Current mirrors (CMs) constitute one of the most basic analog building blocks. To analyze the performance of GC in comparison to Standard SOI nMOSFET in different current mirrors, Common-source, Cascode and Wilson architectures [3], shown in Figure 2, have been studied through two-dimensional circuit simulation and experimental results, as function of the temperature and the L_{LD}/L ratio.

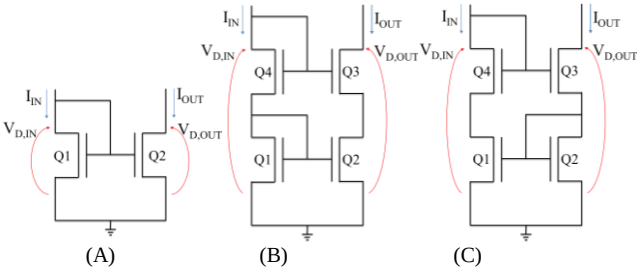


Figure 2 – Common-source (A), Cascode (B) and Wilson (C) current mirror architectures.

In this study, the mirroring precision (P), given by the ratio between the output current and the input current ($P=I_{OUT}/I_{IN}$) and the output resistance $R_{OUT}=\delta V_{D,OUT}/\delta I_{OUT}=1/g_{D,OUT}$ are adopted as figures of merit.

2. PHYSICAL CHARACTERISTICS

The devices that compose the current mirror circuits, indicated in Figure 1, present the following technological parameters: front gate oxide thickness (t_{oxf}) equals to 30nm, silicon film thickness (t_{Si}) equals to 80nm, buried oxide thickness (t_{oxb}) of 390nm and total channel length (L) of 2µm [6]. The L_{LD}/L ratio ranges from zero to 0.75 (this null ratio corresponds to the uniformly doped standard SOI). Moreover, doping concentration levels of the transistors at the source side (N_{AH}), lightly doped side (N_{AL}) and at the source/drain regions (N_D) are equal to $6x10^{16}cm^{-3}$, $1x10^{15}cm^{-3}$ and $5x10^{20}cm^{-3}$, respectively. The characteristics presented above refer to both simulated and measured devices despite of the channel width, which is 20µm in measured transistors and 1µm in the two-dimensional numerical simulations.

3. SIMULATIONS

Sentaurus Device Simulator, from Synopsys, has been chosen to perform all the two-dimensional numerical simulations. This simulator uses the finite element method to solve continuity and Poisson equations [7].

In these simulations, it has been included different models, which describe the carriers' mobility dependencies on the doping concentration level, temperature, normal electric field, velocity saturation of the carriers in high electric fields, dependence of the bandgap narrowing on the doping concentration. As the model responsible for considering impact ionization overestimates this effect, it has suffered adjustments as follow: for electrons, the impact ionization coefficients *a* and *b* have been changed to $7.5x10^5 cm^{-1}$ and $3.5x10^6 cm^{-1}$, respectively, in order to increase the threshold energy for impact ionization [8]. In addition to these models, to simulate devices for temperatures below 300K, it has been included the incomplete ionization effect model.

3.1. Mirroring Precision Simulation

Figure 3 shows the mirroring precision (P) *versus* the normalized input current ($I_{IN}/(W/L_{eff})$) curves for Common-source, Cascode and Wilson CM circuits implemented using Standard SOI ($L_{LD}/L=0$) and GC SOI ($L_{LD}/L=0.5$) transistors, simulated considering $V_{D,OUT}$=1.5V and T=300K. The curves are presented as a function of the normalized input current by (W/L_{eff}) in order to not consider the difference in the dimensions caused by the reduction of the effective channel length in GC devices.

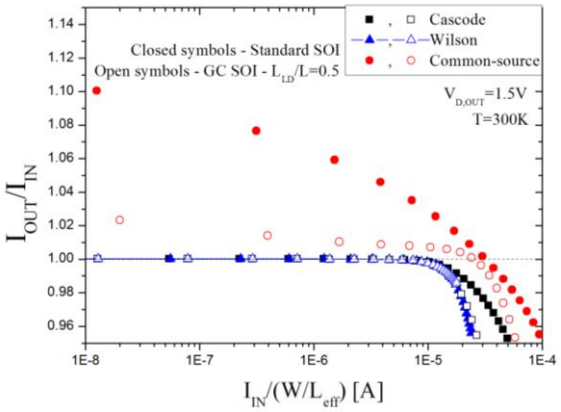


Figure 3 – (I_{OUT}/I_{IN}) vs. ($I_{IN}/(W/L_{eff})$) curves for different CMs with devices of L_{LD}/L=0 and 0.5, $V_{D,OUT}$=1.5V and T=300K.

Figure 3 presents a dashed line at (I_{OUT}/I_{IN}) equals to one that refers to the ideal mirroring precision, since the output and input transistors in the CMs have the same dimensions.

One can note the improvement caused by using Cascode or Wilson CM instead of Common-source circuit and this improvement is so significant that the advantage of using GC cannot be clearly perceived in these curves. On the other hand, in Common-source architecture, GC reveals a better mirroring precision in comparison to Standard SOI. The reason for both improvements, using Cascode/Wilson CM and GC SOI devices, is due to the decreasing of output conductance ($g_D=dI_{DS}/dV_{DS}$) promoted by the later, due to channel length modulation effect [9]. In other words, although V_{DS} does not interfere in P theoretically, differences in V_{DS} among the transistors causes an error in (I_{OUT}/I_{IN}) ratio. This error can be minimized by the reduction of output conductance offered by GC devices or by adding more transistors to the circuit, like Cascode and Wilson CMs, in order to set V_{DS} a fixed value where P is determined (Q1 and Q2 transistors).

Aiming at checking if this trend remains the same at low temperatures (T), the same simulations have been performed at 150K and the results are presented in Figure 4. From this figure, an improvement in P is verified at 150K for Common-source CM, while Cascode and Wilson architectures do not present significant changes from 300K. By using GC, the improvement noted in Common-source is even more significant at 150K and its results are as good as Cascode and Wilson's.

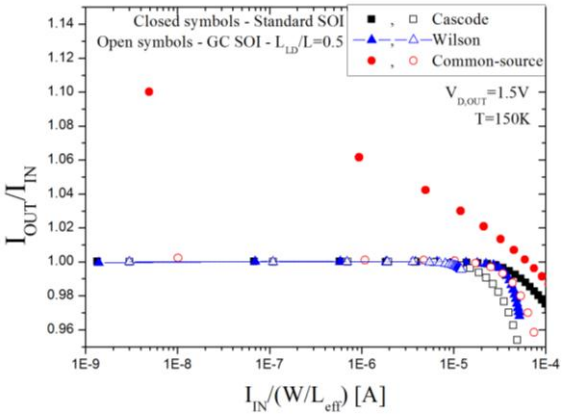


Figure 4 – (I_{OUT}/I_{IN}) vs. ($I_{IN}/(W/L_{eff})$) curves for different CMs with devices of L_{LD}/L=0 and 0.5, $V_{D,OUT}$=1.5V and T=150K.

3.2. Output Resistance Simulation

Aiming to explain the similar characteristics obtained between Cascode and Wilson CMs, Figure 6 shows I_{OUT} versus $V_{D,OUT}$ curves to Cascode and Wilson CMs for Standard and GC SOI devices at 300K.

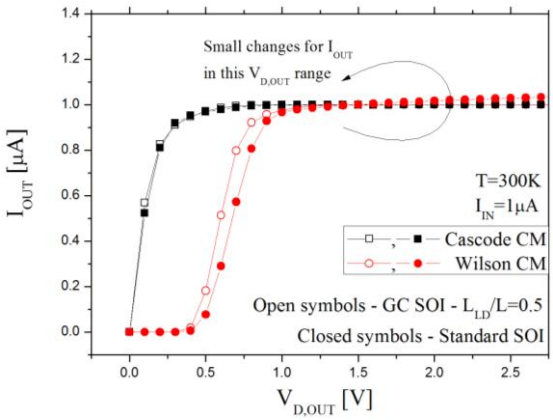


Figure 5 – I_{OUT} vs. $V_{D,OUT}$ curves for Cascode and Wilson of L_{LD}/L=0 and 0.5, I_{IN}=1µA and T=300K.

According to Figure 5, both architectures present small changes in output current for $V_{D,OUT}$ ranging from 1 to 2.5V.

To obtain output resistance, it was performed simulations of the current mirrors with a constant input current equals to 1µA. Then, it was extracted the R_{OUT} from the ($1/g_{D,OUT}$) *versus* $V_{D,OUT}$ curve at $V_{D,OUT}$=2V. Figure 6 presents (R_{OUT}-

/W) *versus* T curves for the current mirror circuits with L_{LD}/L=0, 0.25 and 0.5 for temperature ranging from 150K to 300K with I_{IN}=1µA.

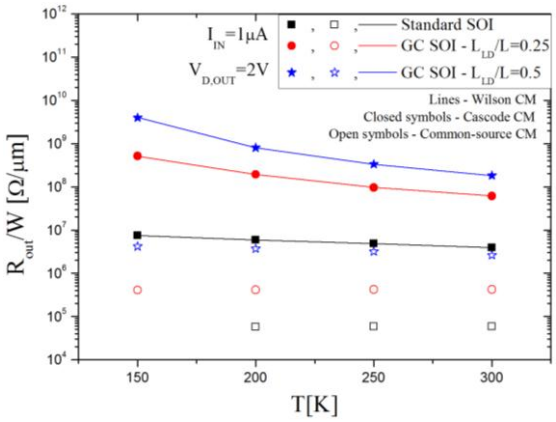


Figure 6 – (R_{OUT}/W) vs. T curves for different CMs with devices of L_{LD}/L=0, 0.25 and 0.5, $V_{D,OUT}$=2V and I_{IN}=1µA.

From Figure 6, one can note that higher output resistances obtained in Graded-Channel CMs with larger L_{LD} are due to the reduction of the output conductance, resultant from the reduction of channel length modulation effect. Besides that, Cascode and Wilson present the same R_{OUT} values, as expected from Figure 5, which are better than Common-source CM. This trend can be verified for all temperature range.

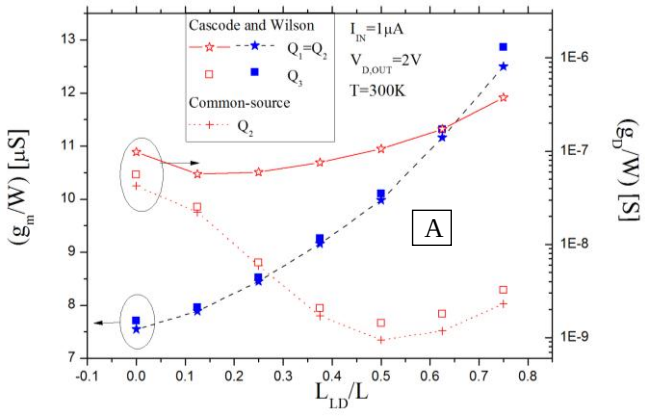
The results obtained for (R_{OUT}/W) extracted from ($1/g_{D,OUT}$) *versus* $V_{D,OUT}$ curves can be confirmed by calculating these values using the expressions (1), (2) and (3) [10]:

$$R_{out} = \frac{1}{g_{D2}} \quad \text{Common-source (1)}$$

$$R_{out} = \frac{g_{m3}}{g_{D2} \cdot g_{D3}} \quad \text{Cascode (2)}$$

$$R_{out} = \frac{g_{m1}}{g_{D1}} \cdot \frac{g_{m3}}{g_{D3}} \cdot \frac{1}{g_{m2}} \quad \text{Wilson (3)}$$

Observing Figure 2, it is possible to note that Q1 and Q2 transistors in Cascode and Wilson CMs have the same polarization, which implies in $g_{m1}=g_{m2}$, $g_{D1}=g_{D2}$ and same results for all parameters between Cascode and Wilson architectures. The results for each parameter in (1), (2) and (3) as function of L_{LD}/L is expressed in Figure 7, to I_{IN}=1µA, $V_{D,OUT}$=2V and T=300K (A) and T=150K (B).



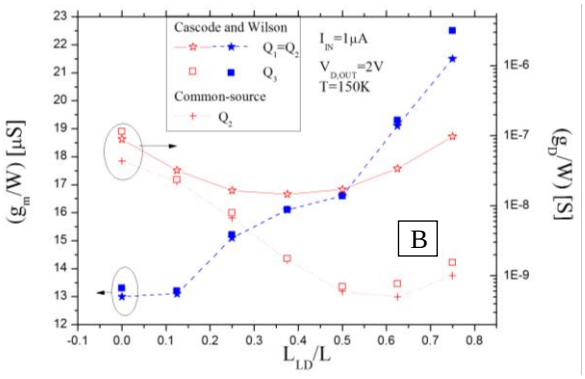


Figure 7 – (g_m/W) and (g_D/W) vs. L_{LD}/L curves for different CMs, $V_{D,OUT}$=2V, I_{IN}=1µA, T=300K (A) and T=150K (B).

These curves express the advantages of GC SOI transistors considering transconductance and output conductance, apart from showing the degradation of g_D and improvement of g_m as temperature gets low. Although g_m always increases with L_{LD}/L increment (due to L_{eff} reduction), g_D degrades from a L_{LD}/L ratio that makes the effective channel length so small that the device suffers short channel effect.

Figure 8 express the output resistance normalized by W as a function of the temperature calculated from the expressions (1) to (3). It is possible to note that the results obtained in Figure 5 and 8 differ in small values.

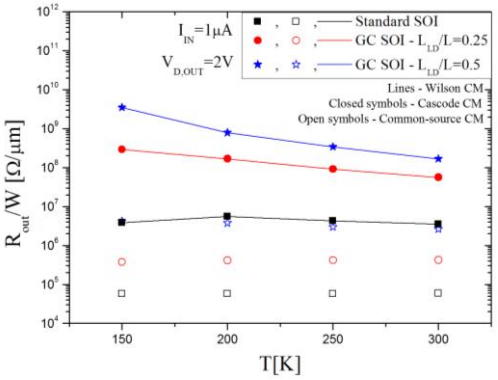


Figure 8 – (R_{OUT}/W) vs. T calculated curves for different CMs, devices of L_{LD}/L=0, 0.25 and 0.5, $V_{D,OUT}$=2V, I_{IN}=1µA.

4. EXPERIMENTAL RESULTS

In order to validate the simulated results presented in this work, experimental data were also measured [3].

The measured curves have been obtained using the Variable Temperature Micro Probe System K20 from MMR Technologies and Keithley 4200 Semiconductor Characterization System.

4.1. Mirroring Precision

Figure 9 presents P *versus* (I_{IN}/(W/L_{eff})) measured curves for Common-source, Cascode and Wilson CMs with Standard SOI transistors and GC SOI devices with L_{LD}/L ratio around 0.5 (the same ratio in simulations of mirroring precision curves), performed at room (A) and low temperatures (B) for a output drain voltage equals to 1.5V.

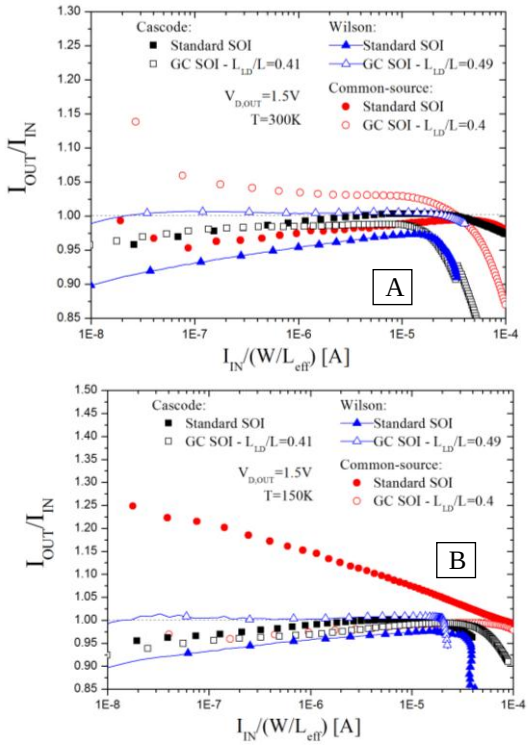


Figure 9 – (I_{OUT}/I_{IN}) vs. ($I_{IN}/(W/L_{eff})$) curves for CMs with Standard and GCs, $V_{D,OUT}$=1.5V, T=300K (A) and T=150K (B).

Measured results present worse results than simulated ones due to intrinsic device mismatch [11] amongst the circuits, once this effect is not observed in simulations. However, it is possible to verify positive changes by using GCs in CMs, whereas temperature variation influence is more perceptible in Common-source architecture.

4.2. Output Resistance

Table 1 shows (R_{OUT}/W) *versus* T measured results for the CMs with Standard and GC SOI devices to temperature raging from 150K to 300K with I_{IN}=1µA.

Table 1 – R_{OUT}/W measured results for Common-source, Cascode and Wilson CMs, $V_{D,OUT}$=2V and I_{IN}=1µA

(R_{OUT}/W) [MΩ/µm]				
Current Mirror Circuit	**Temperature [K]**			
	150K	**200K**	**250K**	**300K**
Common-source CM Standard SOI	0.398	0.393	0.404	0.396
Common-source CM GC SOI - L_{LD}/L=0.40	11.8	11.9	12.2	14.1
Cascode CM Standard SOI	17.1	26.7	37.5	44.0
Cascode CM GC SOI - L_{LD}/L=0.41	51.6	73.0	103	127
Wilson CM Standard SOI	14.8	29.2	34.5	39.2
Wilson CM GC SOI - L_{LD}/L=0.49	57.3	95.8	142.9	156.3

The same trend observed in simulations related to improvements offered by using both Cascode/Wilson CMs and GC SOI devices in the circuits is noted in Table 1. Besides that, analyzing the same CM circuit, R_{OUT}/W values increase up to 2.73 times from 150K to 300K, a small variation considering a logarithmic scale.

5. CONCLUSIONS

This study has shown the particular application of the GC devices in current mirrors demonstrating that this technology keeps better results than uniformly doped devices for mirroring precision and output resistance due to the decreasing of the output conductance. The output resistance depends on the transconductance values as well as the output conductance and the improvement of these parameters provided by Graded-Channel transistors benefits R_{OUT}. Common-source current mirrors presented higher improvements than the others by using GC SOI devices and changing temperature from room to low, because they are more susceptible to drain to source differences, once these circuits have just a couple of transistors. However, mirroring precision results for Cascode and Wilson architectures are not affected visibly, because their extra couple of transistors keeps V_{DS} much less susceptible to differences among the devices.

An important fact related to the benefits brought by GC is that, instead of using Cascode or Wilson CMs, one can use Common-source circuits with GC SOI devices to obtain good results occupying half of the area that the architectures composed by four transistors occupy, in other words, through GC technology, two transistors can execute the same task that four transistors does without significant loss of performance.

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6. REFERENCES

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