Design Methodology for Class E Power Oscillators

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ABSTRACT

In this paper, we present a methodology to design highly efficient class E power oscillators. By combining Hartley oscillator equations and a Class E power amplifier design method, we come up with a set of design equations. Theoretical insight as well as design steps are given. We design a 125 kHz power oscillator prototype using a discrete power MOSFET, achieving a 73 % efficiency at a supply voltage of 2 V.

1. INTRODUCTION

Integrated circuit technology allows for implementing more functions in more compact devices, at a cost of power consumption. On the other hand, the miniaturization of batteries does not follow the same pace, and as a consequence, there is an increasing demand for alternative power supply technologies. Wireless powering of devices comes as one solution to this issue [3]. For instance, remotely-powered circuits have been tested on biomedical implants for non-invasive procedures for either powering devices or recharging batteries [4].

A basic block diagram of a wireless power transfer system is shown in Figure 1. The goal is to transfer energy from the DC source to the load using magnetic coupling. A DC-AC conversion takes place in a block composed by the oscillator and the power amplifier, which is connected to a matching network, responsible for impedance matching with the transmitter inductor. The same occurs on the receiver side, where a matching network couples the inductor L2 to the load.

Efficiency, though, is still a challenging issue in a wireless power system since the energy losses in the overall process can seriously limit any implanted device operation. Usually, the oscillator and the amplifier are implemented as separated circuits, each one contributing for reducing the efficiency of the whole system. A more suitable approach is to design an efficient oscillator which is capable of delivering high power

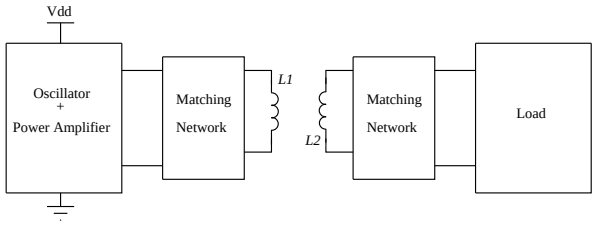

Figure 1: Block diagram of wireless power transfer systems.

to the load without an intermediate amplifier [4]. Among different power oscillator topologies, the class E becomes attractive due to its theoretical high drain efficiency which can be as high as 100 %. A drawback associated to design a class E power oscillator is the lack of an accurate but simple design methodology. For example, the approach presented in [2] is not iterative and requires a complete characterization of the transistor, as well as the procedure found in [4] is based on extensive simulation, making the design arduous and longstanding.

In this paper, we present a straightforward methodology to design class E power oscillators. The proposed methodology is based on the design procedure of class E power amplifiers [1] adapted to a Hartley oscillator topology as found in [4]. The design flow is presented in steps in order to establish a simplified and understandable methodology. In order to validate the methodology, we designed a prototype operating in 125 kHz with $V_{DD} = 2$ V using an IRL540NS power transistor, achieving 73% drain efficiency.

2. CLASS E POWER AMPLIFIER

A power amplifier is responsible for supplying maximum power to the load, as efficiently as possible. Among many topologies found in literature, the class E power amplifier is an interesting alternative due to its 100% theoretical efficiency [7]. The main characteristic of this class of amplifier is to minimize the overlap between current through and the voltage over the transistor drain and source terminals [7]. The typical drain current and voltage waveforms of a class E power amplifier are shown in Figure 2. When there is current across the transistor's source, the drain voltage is zero (the switch is on/closed). When there is voltage between the channel terminals, the current is zero and the transistor is cut off(switch is off/open). In addition, a capacitor placed

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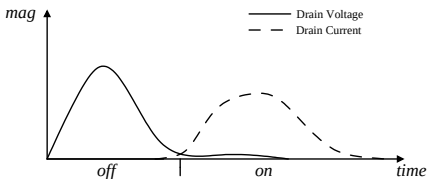

Figure 2: Source current and drain voltage of an ideal Class E amplifier (adapted from [7]).

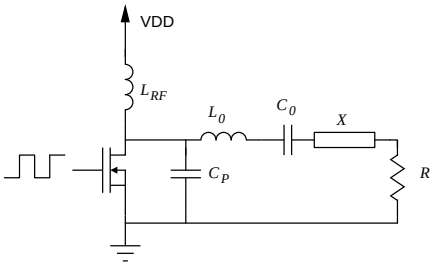

Figure 3: PA Class E circuit schematic.

in parallel with drain and source which forces the drain voltage derivative to be zero at the moment that the transistor switches from off to on state [7].

The Power Amplifier schematic can be seen in Figure 3. In Sokal analysis [7], the inductor L_{RF} serves only as a DC source (RF Choke), but in [1] it is shown that by choosing properly the value of L_{RF}, higher efficiency can be achieved. This paper uses a limited value for L_{RF}, as will be seen later. In order to achieve a sinusoidal current at the output, L_0 and C_0, tuned at the gate signal frequency, must have a high quality factor. X is the excess reactance of the RLC (L_0, C_0 and R) circuit and can be either inductive or capacitive [1].

Method for PA Design

In order to obtain the value of the components of the class E PA, the method presented in [6] and in [7] requires analysis of differential equations. In [4], extensive simulations are required. The method presented in [1] makes possible to obtain the values of all PA circuit components just by solving simple polynomial equations. This is accomplished by choosing the supply voltage (V_{DD}), the operating frequency (w), the load resistance (R) and a parameter q, which is a free design parameter that can be chosen by the designer. By complex mathematical analysis, [1] uses an auxiliary set of coefficient (K_L, K_C, K_P, K_X) to express the components values in terms of q. The values of these auxiliary coefficients in terms of (L_{RF}, C_P, X and R) are expressed in equations below [1]:

$$K_L = wL_{RF} \tag{1a}$$
$$K_C = wC_PR \tag{1b}$$
$$K_P = P_{OUT}R/V_{DD}^2 \tag{1c}$$
$$K_X = X/R \tag{1d}$$

In addition, these coefficients are related to q according to [1]:

$$K_L(q) = 8.085q^2 - 24.53q + 19.23 \tag{2a}$$
$$K_C(q) = -6.97q^3 + 25.93q^2 - 31.071q + 12.48 \tag{2b}$$
$$K_P(q) = -11.90q^3 + 42.753q^2 - 49.63q + 19.70 \tag{2c}$$
$$K_X(q) = -2.9q^3 + 8.8q^2 - 10.2q + 5.02 \tag{2d}$$

Choosing parameter q value

From (1c), we notice that K_P is directly proportional to P_{OUT}, the power delivered to the load R. For our application purpose (energy transfer), it is important to deliver the maximum amount of power to the load for a given load resistance value. This is accomplished by selecting the value of q related to maximum K_P. This value can be calculated by deriving the expression of K_P and setting it to zero. Doing this, we find $q = 1.412$ [1].

By looking at Figure 3, we see that a driver signal is needed. If we consider the circuit required to generate it and its consumed power, the system efficiency decreases significantly from the theoretical 100%. One attractive solution is to build a system that does not require external bias and preserves Class E operation characteristics. This circuit is called a class E power oscillator.

3. CLASS E POWER OSCILLATOR

The oscillator circuit schematic is shown in Figure 4. Using the classical formulation for Hartley oscillators, the oscillation frequency can be expressed as:

$$w = \frac{1}{\sqrt{C_F(L'_{RF} + L'_{Bias})}} \tag{3}$$

Where L'_{RF} and L'_{Bias} are the equivalent inductances seen by the circuit. Hence, considering the extrinsic transistor capacitances, the inductors L_{RF} and L_{Bias} need to have a value such that their inductances seen by the circuit are equal to L'_{RF} and L'_{Bias}. This condition is accomplished by choosing the inductance expressed by:

$$L_{RF} = \frac{L'_{RF}}{1 + w^2 L'_{RF} C_P} \tag{4}$$

$$L_{Bias} = \frac{L'_{Bias}}{1 + w^2 L'_{Bias} C_{GS}} \tag{5}$$

Where C_{GS} is the gate-source capacitance and C_P is the capacitance calculated by the q method. These equations can be found by calculating the parallel equivalent impedance of the inductor and capacitor.

4. POWER OSCILLATOR DESIGN METHOD

Once we have presented the formulation to design the class E power amplifier and the Hartley Oscillator, we can use the same equations to design the class E power oscillator. The basic block that composes the oscillator is presented in Figure 4 (dashed lines). Since we have equations to design both blocks (PA and oscillator), we are able to design the power oscillator just by coupling these equations using the inductor L_{RF} value, which is common to both circuits. The

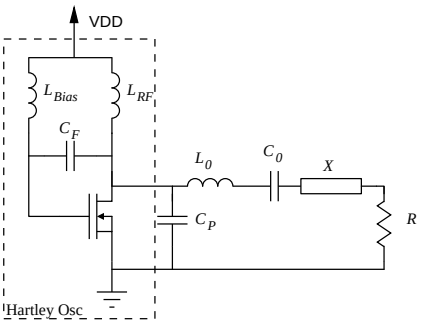

Figure 4: Class E power oscillator circuit schematic.

complete design flow of the design methodology presented in this paper is shown in the steps below.

- **Step 1**: Choose the values of w, V_{DD}, q, R and C_F. For our purpose, $q = 1.412$
- **Step 2**: With the chosen value of q, find the value of K_L, K_C, K_P and K_X using (2).
- **Step 3**: With R and K_L, (1a) gives L'_{RF}.
- **Step 4**: Using the oscillation frequency (3), L'_{RF} and C_F, we obtain L'_{Bias} . Also, we obtain C_P, X and P_{OUT} using the remaining (1b), (1c), (1d).
- **Step 5**: With (4) and (5) and the values of C_P, L'_{RF} and L'_{Bias} we obtain L_{RF} and L_{Bias}.
- **Step 6**: The resonance frequency is expressed as:

$$w = \frac{1}{\sqrt{C_0 L_0}} \tag{6}$$

  Choosing a value for L_0, we can obtain C_0.

Setting parameters V_{DD} and R

Setting Vdd: According to the classical Hartley oscillator formulation, the start up condition can be expressed as:

$$g_m R > \frac{L_{RF}}{L_{Bias}} \tag{7}$$

Where g_m is the transistor transconductance. Hence, V_{DD} must be high enough to bias the transistor and to provide enough g_m so the circuit start oscillating. On the other hand, V_{DD} is up limited to the value in which the lowest value of the gate voltage is above the threshold voltage of the used transistor. If this condition is not satisfied, the transistor, as a switch, will always remain closed and the class E operation conditions can no longer be satisfied since it will always have current flowing through drain to source.

Setting R: By looking again at the classical formulation of Hartley oscillators, it is possible to show, as an oscillation condition, that the reactance X_{RF} and X_{bias} must have the same sign, which is the opposite of the sign of X_F. Since X_{RF} is inductive, by the q method, we need a X_{bias} also inductive. Isolating L'_{Bias} in (3), we obtain:

$$L'_{Bias} = \frac{1 - w^2 C_F L'_{RF}}{w^2 C_F} \tag{8}$$

We need that:

$$L'_{Bias} = \frac{1 - w^2 C_F L'_{RF}}{w^2 C_F} > 0 \tag{9}$$

Or, isolating L'_{RF}:

$$L'_{RF} < \frac{1}{w^2 C_F} \tag{10}$$

Substituting K_L, given by (1a), in (10) and isolating R, we find:

$$R < \frac{1}{K_L w^2 C_F} \tag{11}$$

Which is the upper limit for the load resistance.

After design and simulation, a tuning method can be used in order to achieve higher efficiency. Because of its simplicity, the method used here is the one presented by [5]. For this purpose, [5] shows how to adjust the drain to source voltage in order to decrease the current-voltage overlap between these two terminals.

5. DESIGN EXAMPLE

In this section, the design methodology is verified to design a 125 kHz power oscillator. Here we show step by step the methodology presented in Section 4.

Step 1: At first, we set $Vdd = 2\,\text{V}$, $q = 1.412$, $R = 100\,\Omega$, $C_F = 3.6\,\text{nF}$ and $w = 2\pi 125\,\text{rad/s}$.

Step 2: Now, we compute the coefficients (K_L, K_C, K_P, K_X) using (2) and the results are shown in Table 1:

Table 1: Calculated Coeficients

K_L	K_C	K_P	K_X
0.713	0.685	1.36	−0.00143

Step 3: $R = 100\,\Omega$ and K_L gives $L'_{RF} = 90.78\,\mu\text{H}$, using (1a).

Step 4: w, $L'_{RF} = 90.78\,\mu\text{H}$ and $C_F = 3.6\,\text{nF}$ in (3) gives $L'_{Bias} = 359.52\,\mu\text{H}$. Also, using (1b), (1c) and (1d) we obtain $C_P = 8.31\,\text{nF}$, $X = 8.86\,\mu\text{F}$ and $Pout = 54.4\,\text{mW}$.

Step 5: $L'_{RF} = 90.78\,\mu\text{H}$ and $C_P = 8.31\,\text{nF}$ in (4) gives $L_{RF} = 60.98\,\mu\text{H}$. $L'_{Bias} = 359.52\,\mu\text{H}$ and $C_{GS} = 1.3\,\text{nF}$ in (5) gives $L_{Bias} = 279\,\mu\text{H}$, where C_{GS} is the transistor's gate to source measured capacitance.

Step 6: By choosing $L_0 = 660\,\mu\text{H}$ in (6), we obtain $C_0 = 2.45\,\text{nF}$.

The final values of the calculated parameters and the used ones are shown in Table 2.

The system efficiency was calculated using the following relation:

$$\eta = \frac{Pout}{Pdc} \tag{12}$$

Where $Pdc = Idc \times Vdd$ is the power delivered to the circuit by the DC supply voltage and P_{OUT} is expressed as:

$$Pout = \frac{V_{rms}^2}{R} \tag{13}$$

Table 2: Circuit parameters values

Component	Calculated	Used
L_{RF}	60.98 μH	66 μH
L_{Bias}	280 μH	243 μH
C_F	3.6 nF	3.6 nF
C_P	8.31 nF	8.6 nF
X	8.86 μF	10 μF
C_O	2.45 nF	2.4 nF
L_O	660 μH	660 μH
R	100 Ω	100.5 Ω
q	1.412	1.412
Vdd	2 V	2 V
$Pout$	54.4 mW	54.4 mW

For a sinusoidal output current:

$$Pout = \frac{V_{peak}^2}{2R} \tag{14}$$

In our example, the output power calculated and measured can be seen in Table 3.

Table 3: Results and comparision of Efficiency.

-	This work	[1]	[4]	[2]
$Frequency$	125 KHz	10.24 MHz	6 MHz	800 KHz
Pin	60.3 mW	203.2 mW	21.85 mW	1.157 W
$Pout$	44 mW	171.1 mW	15.85 mW	953 mW
η	72.96 %	84.2 %	72 %	82 %

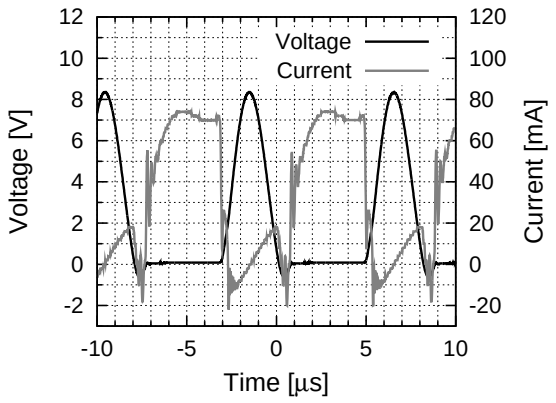

Figure 5: Transistor's drain voltage and source current measured waveforms.

It is important to notice that the values of efficiency shown in this paper considered all circuit losses. A comparison between the results obtained in this paper and results from other papers is presented in Table 3. In [1] an efficiency of 84.2% was achieved, but it did not take into account the power needed to generate the driver signal. In [4], an efficiency of 72% was achieved but extensive simulation was needed. [2] achieved 82 % but the solution of complex equations and transistor characterization was needed.

The difference between the measured efficiency and the 100% theoretical efficiency can be explained by looking at Figure 5. During the transition of the switch(from on to off state) there is some overlap of current and drain voltage, therefore decreasing the system efficiency. Ideally, in order to achieve high efficiency, the gate voltage must be a square waveform [7], making the transition from on to off state as fast as possible. In the used topology, the signal applied to the gate is a sinusoidal waveform, causing the efficiency to decrease. In addition, the difficult to accurately measure the parasitc capacitances of the used transistor may have contributed to decrease efficiency due to components miscalculation.

6. CONCLUSIONS

A complete method to design a power oscillator operating in class E was presented in this paper. By solving simple equations, it was possible to compute all the circuit components without needing extensive adjustments or simulations. The comparision presented in Table 3 shows that the value of 73% achieved in this paper is reasonable if compared to other works, verifying the methodology purposed.

Acknowledgments

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