A NEW MODULE OF THE SWITCHCRAFT TOOL TO INCORPORATE DELAY AND POWER CONSUMPTION ESTIMATION

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ABSTRACT

This work describes the development of a module for delay and power estimation of complex CMOS gates to be integrated with a cell creator tool. The use of analytical models allows fast and accurate estimation of delay power without expensive electrical simulations. The main challenges on developing such module are discussed. The model is still under development.

1. INTRODUCTION

The standard cell approach is largely used in VLSI design. This strategy presents a good time-to-market without being too expensive when compared to a full custom methodology. When compared to programmable logic designs, it presents a better performance and more design flexibility.

For standard cell design is quite useful the availability of CAD tools which are able to fast estimate cell data, without being as expensive as electrical characterization tools.

This paper describes a new tool to estimate delay and power consumption of CMOS gates. The main goal of this work is to integrate analytical models into an automatic cell creator tool in order to improve the characterization process of gates. The runtime is low and the outputs of the tool do not have major discrepancies of precision when compared to electrical simulation data. When integrated with an application that generates automatically transistor networks, such as SwitchCraft [1], it is possible to compare delay and power consumption of logically equivalent functions presenting distinct transistor arrangements.

Some of the estimative models for transistor and node capacitance calculation, can be replaced by other models according to the user preferences. This way, other models can be implemented and compared.

The rest of the text is organized as follows. Section 2 and Section 3 present a brief overview on analytical model for delay and power consumption, respectively. Section 4 discusses transistor networks. Section 5 presents the module implementation. Section 6 presents experimental results, and Section 7 outlines the conclusions.

2. GATE DELAY ESTIMATION

The task of deriving an accurate timing model is quite difficult due to the non-linearity of the circuit behavior, being so the focus of many researches over the years [2-4], and reference therein. The influence of the load capacitance, input transition time, I/O coupling capacitance, short-circuit current, velocity saturation, channel length modulation, drain-induced barrier lowering (DIBL), body effect, and other second order effects represents the main challenge in developing such delay models.

In this work, an arc must be chosen. An arc is defined as the switching of an input signal that results in the output transitioning. According to the arc, an estimative of voltage variation over the capacitances is calculated.

The electric current is estimated using the α-power transistor model [5]. Considering that math analysis of complex gates is very difficult, the proposed tool compress the network.

At the compression, all non-switching transistors are reduced to an electrical equivalent transistor, as shown in Fig. 1.

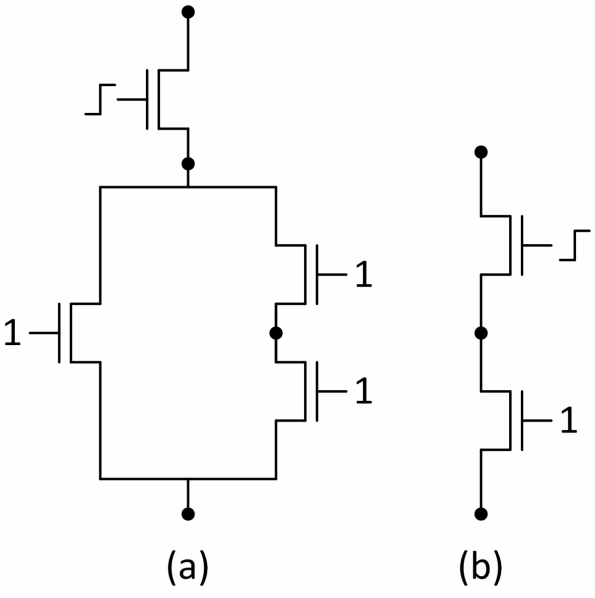

Figure 1- Original (a) and compressed network (b)

Finally, delay is estimated according to the following equation:

$$t = \frac{\sum Ci\,\Delta Vi}{Iavg} \qquad (1)$$

where *Ci* is transistor capacitance, *Vi* is the fall of voltage, and *Iavg* is average current.

3. POWER CONSUMPTION ESTIMATION

There are two power consumption components in CMOS gates. The static consumption, that always occurs when circuit is in steady state, and the dynamic consumption, which can be divided into two components better identified as capacitances charging and short-circuit current.

To estimate intrinsic dynamic consumption of a logic CMOS gate, it is necessary to know the values of the capacitances at intermediate circuit nodes.

For each arc, the initial and the final voltage over the capacitance are calculated. The initial voltage of each node is compared with the final voltage to identify the capacitances that are charged during the output transitioning. As known, NMOS transistor is not a good conductor of logic value "1", and PMOS transistor is not good conductor of logic value "0". In these cases, a correction factor is used to better estimate the power consumption. This correction is used because the voltage variation interval of the capacitances is not actually from "0" to *Vdd*. The variation (voltage swing) is from "0" to *Vdd* - *Vtn* in NMOS transistors, and from *Vdd* to "0" + *Vtp* in PMOS transistors. The final energy is calculated based on the equation:

$$E = \sum C_{nodo} \times {V_{DD}}^2 \qquad (2)$$

To estimate the static power consumption, the SwichtCraft [1] tool uses the method presented in [6]. For each possible input vector, the leakage current of the logic gate is estimated. To predict the electric current, the subthreshold current and the gate oxide current are considered, as well as the interaction between them.

4. TRANSISTOR NETWORKS AND CMOS LOGIC GATES

Static CMOS logic gates are composed of pull-up (PU) network with PMOS transistors connecting the output to the power node (Vdd), and a pull-down (PD) network with NMOS transistors connecting the output to the ground node (Gnd).

A network can have series or parallel switches. Networks with series switches turn on when all transistors are turned on. Networks with parallel switches turn on when at least one transistor is turned on.

Using the networks described above is possible to implement any logic function. The generic schematic of a logic gate is shown in Fig. 2 [7].

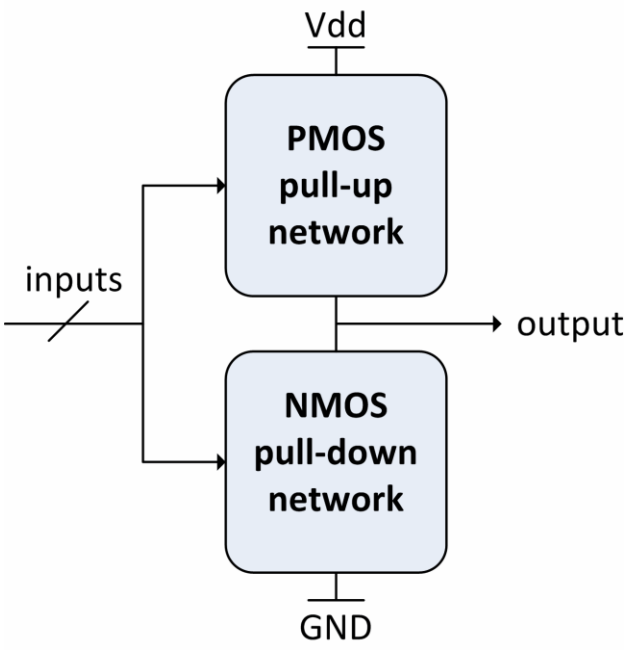

Figure 2- Generic schematic of a conventional static CMOS logic gate

5. PROPOSED MODULE FOR SWITCHCRAFT

In this section an implementation overview of some algorithms used at the tool is given.

5.1. Internal Capacitances

Capacitances in MOS transistors can be divided into gate capacitance (*Cg*), depletion capacitances (*Cdb* and *Cds*) and overlap capacitances (*Cgd* and *Cgs*), as shown in Fig. 3a. The model used in this work is shown in Fig. 3b [8].

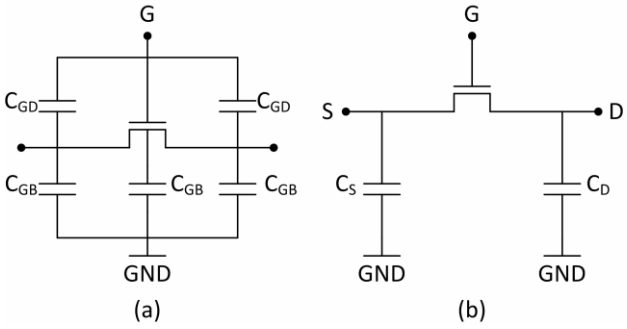

Figure 3- Capacitance model: (a) MOSFET and (b) simplified approach.

The drain and source intrinsic equivalent capacitances are defined as follow:

$$Cd = Cdb + Cgd \qquad (3)$$

$$Cs = Csb + Cgs \qquad (4)$$

Cgd and *Cgs* are obtained from gate capacitance, as shown in the following equation:

$$Cg = Cox \ . \ W \ . \ L \quad (5)$$

where *Cox* is the gate capacitance for area unit. For the estimative, *Cgd* and *Cgs* are defined as:

$$Cgd = Cgs = ½ \ Cg \quad (6)$$

To determine the depletion capacitance, the following LTI (linear time invariant) model is applied:

$$Cdep = CbotAvg + CsidewallAvg \quad (7)$$

where *CbotAvg* is the bottom capacitance of source/drain regions. *CsidewallAvg* is the sidewall capacitances of source/drain region. The average values of these components are calculated by the following equations:

$$CbotAvg = k(v1,v2) \ . \ Cjo \ . \ A \quad (8)$$

$$CsidewallAvg = k(v1,v2) \ . \ Cjosw \ . \ P \quad (9)$$

where *k* is a constant value that is defined according to technological parameters and node voltage variation range. *Cjo* and *Cjosw* are technological parameters. *P* is the source/drain perimeter, and *A* is the diffusion area.

This way, it is possible to calculate the output capacitance of the logic gate adding the capacitances values that are connected to the output node.

5.2. Arcs

To determine a transition arc, minterms and maxterms of the function are analyzed. The Hamming distance between each minterm and maxterm is calculated. If the Hamming distance is 1 then the truth table line corresponds to a possible arc.

5.3. Static Voltage

To estimate static voltage, the algorithm walks through turned on switches in the network. The reference nodes have initial values "1" for *Vdd* and "0" for *Gnd*. Starting at them, a voltage is induced from one node to another, according to MOS transistor type. All switches are bidirectional.

If two different values are induced at the same node, an alert or error is shown.

5.4. Series-Parallel Compression

The compression starts at reference nodes, walking through the network until input switching transistor. At each compression, two series or parallel transistors are replaced by an equivalent transistor. W and L equivalent values are calculated for each compression.

6. EXPERIMENTAL RESULTS

The module is still under development. Nevertheless, all steps discussed in Section 5 have already been individually implemented and verified. Preliminary data are being written in the liberty format. The steps missing are integrating all the steps in a single flow and implementing some mathematical equations.

7. CONCLUSION

This work described a module for delay and power consumption estimation. The integration of this module with SwitchCraft tool [1] allows comparison of transistors networks and fast generation of standard cell libraries. The use of analytical models improves the total runtime while maintaining good accuracy when compared to an electrical simulator such as HSPICE. Moreover, different models can be incorporated into the module. The main challenges on developing the module were discussed, and future work will evaluate the use of the proposed module on a standard cell library flow.

8. ACKNOWLEDGMENTS

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