Energy Evaluation of Nanometer CMOS Technologies

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ABSTRACT
Power consumption becomes a very important constrain integrated circuit designs. Researches propose numerous techniques for achieving low power, on several different levels of abstraction. One of the more efficient approaches is design the circuits with transistors operating in subthreshold or near-threshold region. Its impact on system design is an exponential reduction in power consumption at the cost of reduced performance. This work proposes an evaluation of the effects on energy consumption (static and dynamic) of the subthreshold operation approach when applied to sub 45nm CMOS technologies. Moreover, this work explores the subthreshold operation approach to define how much energy consumption is possible to reduce when the system require medium- throughput (10MHz) and low throughput (100kHz) frequencies. Results show that static energy gains even more importance at low throughput and is a constraint to nanometer technologies.

Categories and Subject Descriptors
B.7.1 **[Hardware]:** Integrated Circuits - *Types and Design Styles*

General Terms
Measurement, Performance, Design.

Keywords
Energy, Low Power, Subthreshold, Nanometer Technologies, CMOS, Inverter, Static Energy.

1. INTRODUCTION
The dimension of the device in VLSI technology has scaled down significantly for the last years. The transistor scaling in each new CMOS technology generation has provided continual improvements in integrated circuits performance and functionalities, reducing the cost per function.

In the past, only specific markets required low-power integrated circuits. The main goal of designers always was achieve the better performance with acceptable power and area. For the last years, there was an explosive growth in portable systems, like mobile phones, wireless sensor, medical electronics tablets and smartphones. Since the capacity of the batteries of those portable electronic products are limited, the power consumption becomes a very important constrain to designers, and increases its importance as research area in microelectronics.

The researches propose numerous techniques for achieving low power, on several different levels of abstraction [1-4]. One of the more efficient approaches is design the digital circuits with transistors operating in subthreshold or near-threshold region [2]. In subthreshold designs, the subthreshold current provides a near ideal voltage transfer characteristics of the logic gates. Its impact on system design is an exponential reduction of power consumption at the cost of reduced performance [2].

In micrometer designs, the static current is usually ignored due to its insignificant value when compared to dynamic power. The device dimension scaling increases the electric field between transistor structures increasing the magnitude of these static currents [5]. In modern designs, if none leakage reduction technique are applied, the static power can respond for more than 50% of total power consumption [6].

In [7], Bol et al. presented a widespread investigation about the impact of technology scaling on digital subthreshold circuits, considering CMOS technologies from 250nm to 32nm. This work highlights that reduction of the technology node imposes limits in the reduction of static energy consumption, i.e., results in a loss of energy efficiency. This statement is supposed to 32nm CMOS predictive technology nodes, and the results show that is possible to improve the energy efficiency adopting a non minimum channel length in the designs.

In complement to this idea, this work proposes an evaluation of the effects on energy consumption (static and dynamic) of the subthreshold operation approach when applied to sub 45nm CMOS technologies. Transistors at same technology node with different threshold voltage are also explored. The transistors with lower threshold voltage are named High Performance (HP), while the ones with higher threshold voltage are the Low Power (LP). The main objective in this analysis is verifying if the behavior reported in previous work [7] is founded in these advanced CMOS technologies. For this propose, predictive models of 45nm, 32nm, 22nm and 16nm CMOS technologies [8] are adopted to design, simulate and evaluate the characteristics of CMOS inverters. Another important contribution of this work is the exploration of how much is possible to reduce the energy consumption when operating in medium- throughput (10MHz) and low throughput (100kHz) with the subthreshold operation approach.

Next section briefly reviews the energy concepts in CMOS circuits. The methodology used in this work is described in Section 3. Section 4 shows the simulation results and analysis. Finally, Section 5 presents the conclusions.

2. ENERGY IN CMOS CIRCUITS
The concept of energy in CMOS circuits reflects the total energy that is spending to realize some computation. The energy per operation in digital CMOS circuits can be decomposed in two parts, which are summarized in the following equation:

$$E_{total} = E_{dynamic} + E_{static} \quad (1)$$

The first term represents the dynamic component of energy. This portion is presented in equation (2).

$$E_{dynamic} = N_{sw}.W_{min}.C_L.V_{dd}^2 \quad (2)$$

Where N_{sw} is the number of switched nodes to perform the operation, W_{min} the minimum device width, C_L the typical load capacitance per width unit and V_{dd} is the applied voltage.

Energy static, E_{static} , is modeled by the following equation:

$$E_{static} = V_{dd}.I_{static}.Delay \quad (3)$$

Where I_{stat} is the leakage current flowing through the devices and *Delay* is the period of the throughput.

3. METODOLOGY

To evaluate nanometer technologies to design low power circuits, this work simulates a CMOS inverter circuit in different technologies and compares the energy results. As mentioned in Section 1, the circuits are designed with two different types of transistors: a low-power (LP) and a high-performance (HP). All results are obtained using the electrical simulator NGSPICE [9]. Eight predictive CMOS technology models are used in this analysis: 45nm HP, 32nm HP, 22nm HP, 16nm HP, 45nm LP, 32nm LP, 22nm LP and 16nm LP [10].

Seeking a simulation closer to reality, the circuit under evaluation is connected to input and output buffers. All inverters has the same sizing, with $W_n = 2L$ and $W_p = 2W_n$. Where L is the minimum length of device technology, W_n is the width of NMOS transistor and W_P is the width of PMOS device. All results take into account only the energy consumed by the circuit under evaluation, i.e., a different font is adopted to supply the main inverter.

The adopted strategy to reduce power is the power-driven voltage scaling, reducing supply voltage and forcing transistors to operate in the subthreshold region (supply voltage V_{dd} less than the transistor threshold voltage V_{th}) [12]. Table 1 presents nominal (V_n), threshold (V_{th}), and subthreshold (V_s) voltages used for each technology node. The transistor threshold voltage has been extracted from I_{ds} x V_{gs} curve. In all simulations the V_{dd} value starts with the nominal value and is reduced to subthreshold value.

Also, this work evaluates the circuits operation with nominal and subthreshold voltages in a medium throughput (frequency of 10MHz) and in a low throughput (frequency of 100kHz). Only low throughput results are compared between transistor types HP and LP, because this is the case where HP presents the worst constraint when considering static energy.

For each inverter in a different technology, total energy and static energy are measured. The total energy was obtained by the equation (4), where t is the period relative to input operating frequency. During this time, the input performs two transitions.

$$E_{total} = \int I(t).V.dt \quad (4)$$

To calculate the static energy, the two logical states possible of the inverter circuit were simulated. Static energy presented in the results is calculated as the average result.

Table 1 - Technologies' Features

Technology	V_n (V)	V_{th} (V)	V_s (V)
45nm HP	1,0	0,357	0,3
32nm HP	0,9	0,335	0,3
22nm HP	0,8	0,334	0,3
16nm HP	0,7	0,256	0,2
45nm LP	1,1	0,624	0,5
32nm LP	1,0	0,616	0,5
22nm LP	0,95	0,614	0,5
16nm LP	0,9	0,572	0,5

4. RESULTS

Firstly, this Section presents the energy evaluation for High Performance designs.

Figure 1 presents the total energy per operation in medium throughput for nominal and subthreshold voltage. The graph shows that by reducing the supply voltage, the total energy per operation falls on average an order of magnitude, achieving two orders in 16-nanometers CMOS technology.

The static energy in medium throughput is exhibited in Figure 2. This component has the characteristic that the static energy increases as the technology node reduce at nominal and subthreshold voltages. The static component exceeds 90% of total consumption in 16 nanometer technology.

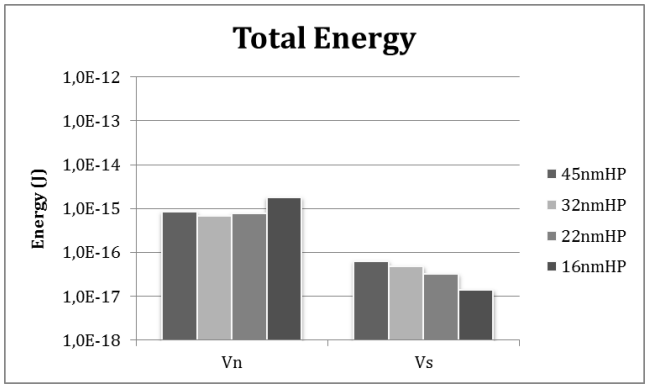

Figure 1 - Total Energy per Operation in HP technologies

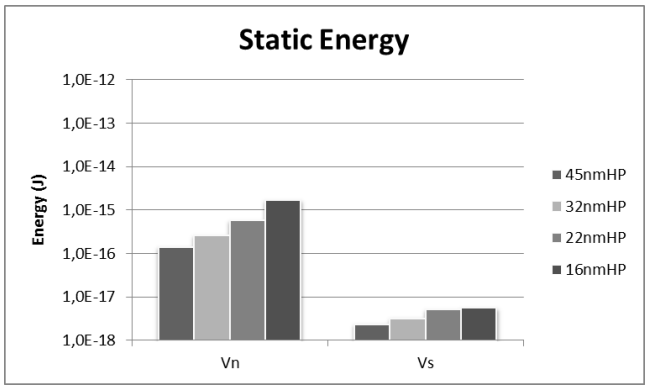

Figure 2 - Static Energy per Operation in HP technologies

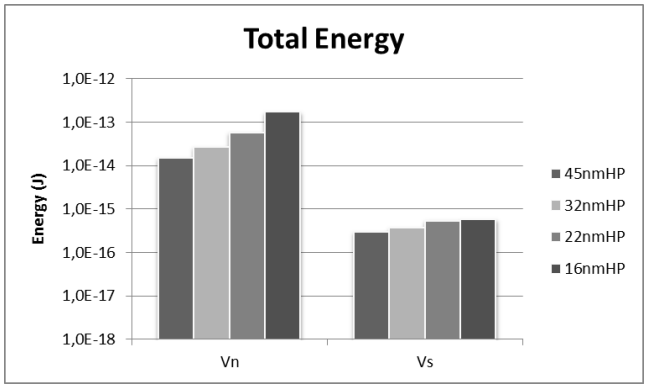

Figure 3 - Total Energy per Operation in Low Throughput

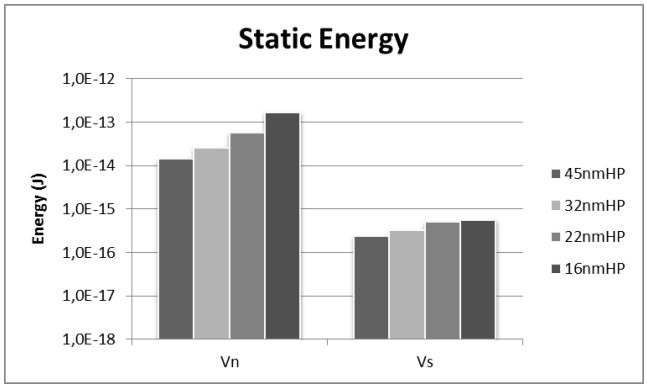

Figure 4 - Static Energy per Operation in Low Throughput

Figure 3 presents the total energy per operation in low throughput, i.e., at 100kHz. Note that energy values are higher at 100khz than at 10MHz (medium throughput). It is because the execution period is longer at low throughput, with the same number of switches performed, thus, dynamic energy remains approximately the same, but static energy is much higher, as displayed in Figure 4. In low throughput, inverter circuits with HP devices have almost all their energy composed by static component, which is shown in Table 2. In this case, even in the technology of 45 nanometers, the static consumption exceeds 90%.

Finally, results for low power technologies are compared to high performance energy data. In contrast to previous data, the evaluation of the inverters in Low Power models shows a lower static current, which makes the dynamic component the major portion of energy consumption. This can be verified in Figures 5 and 6 and in Table 3. Figure 5 shows the total energy per operation in low throughput for designs with LP devices. Comparing with HP results, the total energy is less than one order of magnitude at nominal voltage operation. In subthreshold operation, total energy reduces as the technology node reduces.

Considering static current, LP devices comproves its efficiency and the static power is less than two orders of magnitude of HP designs. It is important to note that, similar to HP results, at nominal voltage the static energy is the main part of total energy in LP systems. However, in subthreshold operation, static energy reduces its impact in total energy, and dynamic energy return to be the main contribution in the total energy.

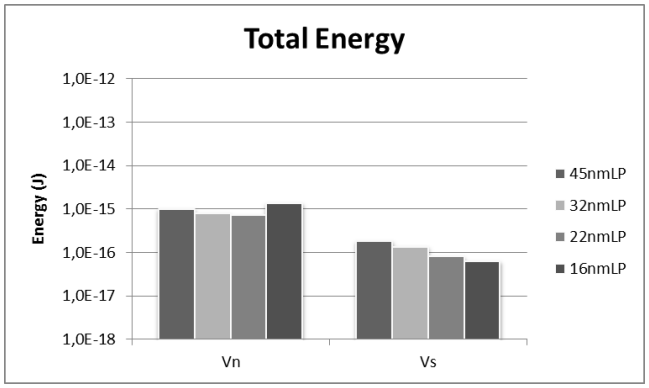

Figure 5- Total Energy in Low Throughput LP Technologies

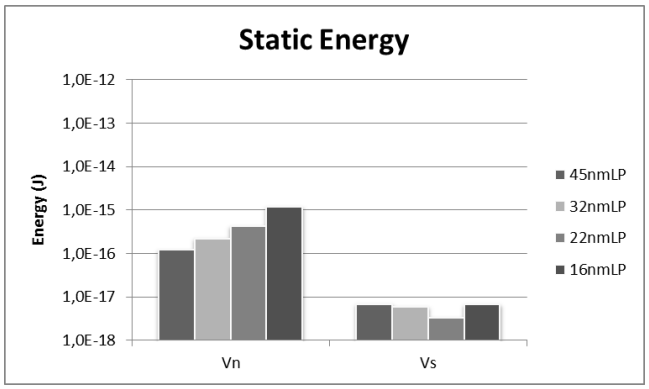

Figure 6 - Static Energy in Low Throughput LP Technologies

Table 2 - Energy in Medium Throughput x Energy in Low Throughput

	Medium Throughput - 10MHz								**Low Throughput – 100kHz**							
	45nmHP		**32nmHP**		**22nmHP**		**16nmHP**		**45nmHP**		**32nmHP**		**22nmHP**		**16nmHP**	
	V_n	**V_s**	**V_n**	**V_s**	**V_n**	**V_s**	**V_n**	**V_s**	**V_n**	**V_s**	**V_n**	**V_s**	**V_n**	**V_s**	**V_n**	**V_s**
E_{total} (fJ)	0.86	0.06	0.68	0.05	0.78	0.03	1.83	0.01	15.1	0.30	26.8	0.37	58.6	0.55	172	0.58
E_{static} (fJ)	0.14	0.002	0.26	0.003	0.58	0.005	1.72	0.006	14.4	0.24	26.3	0.33	58.3	0.52	172	0.56
E_{dyn} (fJ)	0.72	0.06	0.42	0.05	0.19	0.03	0.12	0.009	0.71	0.06	0.49	0.05	0,36	0.03	0,7	0.02
E_{dyn} (%)	83.3	96.3	61.5	93.3	25.3	83.9	6.49	60.7	4.7	21.0	1.85	12.2	0.61	5.19	0.41	3.94

Table 3 - Energy in Low Throughput

	45nmHP		32nmHP		22nmHP		16nmHP		45nmLP		32nmLP		22nmLP		16nmLP	
	V_n	V_s	V_n	V_s	V_n	V_s	V_n	V_s	V_n	V_s	V_n	V_s	V_n	V_s	V_n	V_s
E_{total} (fJ)	15	0.3	27	0.37	59	0.55	170	0.58	1	0.19	0.79	0.14	0.72	0.08	1.4	0.06
E_{static} (fJ)	14	0.24	26	0.33	58	0.52	170	0.56	0.12	0.007	0.23	0.006	0.44	0.003	1.2	0.007
E_{dyn} (fJ)	0.71	0.06	0.49	0.05	0.36	0.03	0.7	0.02	0.89	0.18	0.57	0.13	0.28	0.08	0.18	0.01
E_{dyn} (%)	4.7	21	1.8	12.2	0.6	5.2	0.4	3.9	87.8	96.3	71.6	95.5	39	95.8	12.9	89.3

5. CONCLUSIONS

The results analysis confirms the importance of static consumption on nanometer technologies, mainly when the circuit remains a long time without transitions, i.e., at low throughput. An alternative to minimize the static energy is to use low power devices rather than high performance ones. Evaluating the technologies, as the scaling advance, the CMOS technologies have lower dynamic energy and higher static energy. This behavior represents a constraint to technology scaling, if the application remains idle for a long time. In subthreshold operation, the behavior of inverters is the same, but the dynamic and static energy are significantly lower. As future work, these analyses will be extended to a set of circuits, in order to confirm the presented evaluations.

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