# A 40 mV/4 uW CMOS Colpitts Oscillator with Additional Positive Feedback at 2.12 GHz

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## ABSTRACT

In this paper, a different topology for ultra-low voltage oscillators is presented. It is based on a classical common-gate Colpitts Oscillator, but with additional positive feedback provided by an inductive gate degeneration. This increase in the positive feedback decreases the required transconductance in order to start-up the circuit, which is used here to reduce the minimum supply voltage. The capacitor ratio of the circuit is also optimized with the same purpose. The equations for the optimization are presented as well as a step-by-step design. A prototype with the aim of validate the work was developed in a standard 0.13 $\mu$m CMOS process using a zero-threshold transistor. The post-layout simulation resulted in a minimum supply voltage of 40 mV at 2.12 GHz, with a power consumption of 4 $\mu$W.

## Keywords

Ultra-low voltage, Ultra-low power, CMOS Colpitts Oscillator

## 1. INTRODUCTION

Circuits for Wireless Body Area Networks (WBAN) and Wireless Sensor Networks (WSN) usually have a limited power budget as well as the need for operating with low supply voltages. These circuits are composed, among other blocks, by oscillators. Thus, it is necessary to optimize those blocks in order to work in such conditions.

Several topologies [1, 2, 3, 4] have presented different techniques in order to reduce the supply voltage. In [1] an approach that consists in optimizing the capacitor ratio is presented, which allows the circuit to work with supply voltages as low as 20 mV. [2] presents a technique that allows the signal to swing beyond the supply voltage and GND, therefore decreasing the phase noise while working with low-voltage. In [3] two main techniques are utilized: the use of a capacitor feedback in addition to the negative resistence of a cross-coupled pair of transistors, as well as forward-body-bias technique to reduce the threshold voltage. And finally in [4] it is used a transformer positive feedback with optimization of the turns ratio of the coupled inductors, that allows the circuit to operate below the threshold voltage.

In this paper we present the analysis and design of an ultra-low-voltage oscillator based on the common-gate Colpitts oscillator. By increasing the positive feedback with an inductive gate degeneration, the required transconductance to oscillate is reduced, what allows to apply a lower supply voltage. The analysis for this new positive feedback is developed as well as the optimization of the capacitor ratio. An analytical expression to estimate the critical supply voltage for this topology is also presented. A step-by-step design is developed, as well as a prototype with the aim of proof of concept. The post-layout simulation results are also presented.

## 2. LOW-VOLTAGE OSCILLATOR

The Colpitts oscillator can be analysed as an unstable one-port terminated by a load, as we can see in Figure 1, where $Y_1$ and $Y_2$ are the input admittances of the one-port network and the load, respectively . In order to oscillate the circuit must satisfy the Barkhausen criterion for this case [5]:

$$\Re\left(Y_1\right) \leq -\Re\left(Y_2\right) \tag{1a}$$

$$\Im\left(Y_1\right) = -\Im\left(Y_2\right) \tag{1b}$$

There are several techniques for low-voltage operation of oscillators. One classically employed [1, 2, 3, 4] is the degeneration of the current source into an inductor shown in Figure 2 as $L_{RFC}$. There are two main advantages in the application of this technique: a) all the supply voltage is applied over the transistor therefore increasing the small-signal gain; and b) the inductor allows the signal to swing below the GND potential. The later allows to increase the output amplitude and the output power, thus decreasing the phase-noise [2].

Another technique is the optimization of the capacitor feedback [1, 3]. In our topology, we optimize this parameter to decrease the required transconductance in order to start-up the oscillator. As a result, the supply voltage can be reduced.

The last technique employed here consists in a gate degeneration developed by $Z_g$ in Figure 2a. For the special case $Z_g = j\omega L_g$, and for a suitable value of $L_g$, there is an increasing in the positive feedback, which reduces the minimum supply voltage.

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## 3. CIRCUIT ANALYSIS

We focus our analysis in the reduction of the supply voltage. To that purpose, our analysis is based on the already-developed equations in [1], for the case where $Z_g = 0$ in Figure 2a. We now extend those results for a generic impedance $Z_g$, and for an inductive impedance $Z_g = j\omega L_g$.

### 3.1 General Analysis

The AC equivalent circuit for Figure 2a is shown in Figure 3a. By replacing the transistor small-signal model we obtain the equivalent circuit shown in Figure 3b. We consider $C_{gd}$ in order to make this analysis valid for all the regions of operation [6], though it is more significant for the linear region, which is our case. One could do this analysis for a saturated transistor without considering the intrinsic $C_{gd}$ in order to reduce the complexity of the equations.

We now transform the circuit from Figure 3b into an equivalent one, shown in Figure 3c that was already optimized in [1]. First of all, by superposition we can relate the gate voltage ($v_g$) to the source ($v_s$) and drain ($v_d$) voltages as:

$$v_g = \alpha v_d + \beta v_s \tag{2}$$

where $\alpha$ and $\beta$ are given in Table 1 for a generic impedance $Z_g$, and for the special case $Z_g = j\omega L_g$.

Secondly, the T-network given by $C_{gs}$, $C_{gd}$ and $Z_g$ (see Figure 3b) can be transformed in an equivalent $\pi$-network. The transformation is shown in Figure 4 [7]. Using (2) and the network transformation, we can redraw Figure 3b to obtain the simplified circuit shown in Figure 3c, where:

$$g_{m1} = g_{ms} - \beta g_{mg} \tag{3a}$$

$$g_{m2} = g_{md} + \alpha g_{mg} \tag{3b}$$

$$C_{1eq} = \frac{1}{j\omega Z_{C_1} \,||\, Z_c} \tag{3c}$$

$$C_{2eq} = \frac{1}{j\omega Z_{C_2} \,||\, Z_b} \tag{3d}$$

$$L_{eq} = \frac{Z_{L_1} \,||\, Z_a}{j\omega} \tag{3e}$$

where $Z_a$, $Z_b$ and $Z_c$ are given in Table 1 for a generic impedance $Z_g$, and for the special case $Z_g = j\omega L_g$.

The circuit shown in Figure 3c was optimized in [1] for the minimal supply voltage. Using those results and writing the gate transcondutance as $g_{mg} = (g_{ms} - g_{md})/n$ [6], the minimum source transconductance, $g_{ms}$, necessary to oscillate is:

$$g_{ms} = g_{md} + \frac{g_{md} n \frac{C_{2eq}}{C_{1eq}}}{\gamma}\left(1 + \frac{G_P}{g_{md}}\left(1 + \frac{C_{1eq}}{C_{2eq}}\right)^2\right) \tag{4}$$

where $g_{md}$ and $n$ are the drain transconductance and the slope factor of the transistor, respectively, $G_P$ is the equivalent parasitic conductance of the passive devices, and $\gamma = n - \beta - \alpha(1 + C_{2eq}/C_{1eq})$. This equation is valid for $g_{ms} << \omega(C_{1eq} + C_{2eq})$.

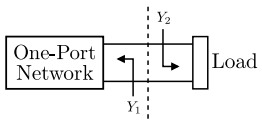


**Figure 1: High-level representation of the oscillator.**

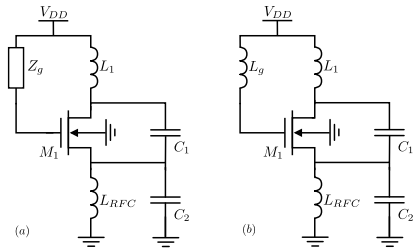


**Figure 2: Proposed topology with (a) a generic degeneration $Z_g$ and (b) an inductive degeneration $Z_g = j\omega L_g$.**

An expression for the minimum supply voltage was also developed in [1]. Extending it for our case, we have:

$$V_{DD}|_{crt} = \phi_t ln\left(1 + \frac{n\frac{C_{2eq}}{C_{1eq}}}{\gamma} + \frac{G_P}{g_{md}}\frac{n\left(1 + \frac{C_{2eq}}{C_{1eq}}\right)^2}{\frac{C_{2eq}}{C_{1eq}}\gamma}\right) \frac{{\phi_t}^2}{2I_S}\frac{g_{md} n \frac{C_{2eq}}{C_{1eq}}}{\gamma}\left(1 + \frac{G_P}{g_{md}}\left(1 + \frac{C_{1eq}}{C_{2eq}}\right)^2\right) \tag{5}$$

where $\phi_t$ is the thermal voltage, and $I_S$ is the specific current of the transistor.

The oscillation frequency for this new topology is given by:

$$f_o = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \tag{6}$$

where $L_{eq}$ is given by (3e), and $C_{eq}$ is given by: $C_{eq} = C_{1eq}C_{2eq}/(C_{1eq} + C_{2eq})$, where $C_{1eq}$ and $C_{2eq}$ are given by (3c) and (3d), respectively.

And finally, by minimizing (4) in relation to $C_{2eq}/C_{1eq}$, we obtain the optimum capacitor ratio $K_{opt}$ in order to reduce the required transconductance as:

$$K_{opt} = \left.\frac{C_{2eq}}{C_{1eq}}\right|_{opt} = \sqrt{\frac{G_P}{G_P + g_{md} + \alpha g_{mg}}} \tag{7}$$

### 3.2 Special Case

A method to reduce the supply voltage is to increase the coefficient $\gamma$ in (5), which depends on $\alpha$ and $\beta$. If we choose those coefficients negatives, the higher we choose them the smaller is the supply voltage. Assuming that the aspect ratio of the transistor and the supply voltage are fixed, and hence the parameters $C_{gs}$ and $C_{gd}$ are fixed, the impedance $Z_g$ is the only parameter that we can change, in order to set $\alpha$ and $\beta$ negative values.

As we can see from Table 1, choosing $Z_g = j\omega L_g$, and setting a suitable value for $L_g$, we can set both $\alpha$ and $\beta$ negatives. The condition for $L_g$ is:

$$L_g < \frac{1}{\omega^2\left(C_{gs} + C_{gd}\right)} \tag{8}$$

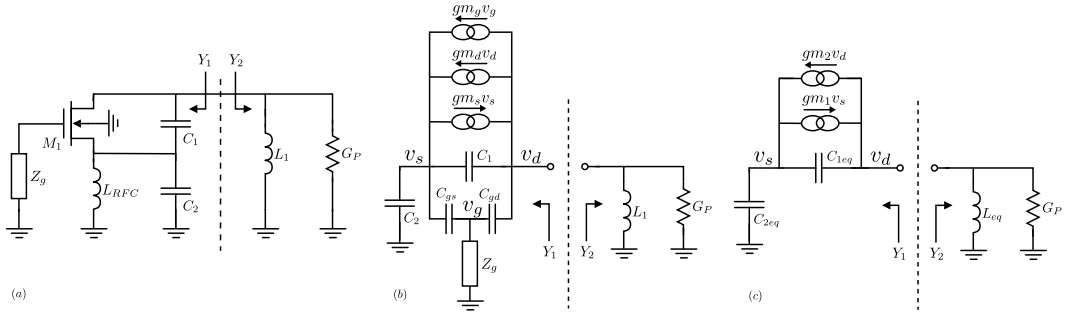


**Figure 3: (a) AC equivalent circuit, (b) small-signal and (c) simplified small-signal representation.**

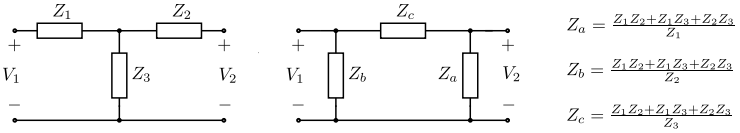


**Figure 4: T to $\pi$ network transformation**

**Table 1: Coefficient Values for the general case and for the special case when $Z_g = j\omega L_g$.**

| Coefficient | General Value | Special Value($Z_g = j\omega L_g$) |
|---|---|---|
| $\alpha$ | $\frac{Z_{C_{gs}} \| Z_g}{Z_{C_{gs}} \| Z_g + Z_{C_{gd}}}$ | $\frac{1}{1+\frac{C_{gs}}{C_{gd}} - \frac{1}{\omega^2 L_g C_{gd}}}$ |
| $\beta$ | $\frac{Z_{C_{gd}} \| Z_g}{Z_{C_{gd}} \| Z_g + Z_{C_{gs}}}$ | $\frac{1}{1+\frac{C_{gd}}{C_{gs}} - \frac{1}{\omega^2 L_g C_{gs}}}$ |
| $Z_a$ | $\frac{Z_{C_{gs}} Z_{C_{gd}} + Z_{C_{gs}} Z_g + Z_{C_{gd}} Z_g}{Z_{C_{gs}}}$ | $j\omega C_{gs}\left(\frac{L_g}{C_{gs}} + \frac{L_g}{C_{gd}} - \frac{1}{\omega^2 C_{gs} C_{gd}}\right)$ |
| $Z_b$ | $\frac{Z_{C_{gs}} Z_{C_{gd}} + Z_{C_{gs}} Z_g + Z_{C_{gd}} Z_g}{Z_{C_{gd}}}$ | $j\omega C_{gd}\left(\frac{L_g}{C_{gs}} + \frac{L_g}{C_{gd}} - \frac{1}{\omega^2 C_{gs} C_{gd}}\right)$ |
| $Z_c$ | $\frac{Z_{C_{gs}} Z_{C_{gd}} + Z_{C_{gs}} Z_g + Z_{C_{gd}} Z_g}{Z_g}$ | $\frac{1}{j\omega L_g}\left(\frac{L_g}{C_{gs}} + \frac{L_g}{C_{gd}} - \frac{1}{\omega^2 C_{gs} C_{gd}}\right)$ |

Note that for the limit case of (8), the coefficients $\alpha$ and $\beta$ tends to minus infinity, the required source transconductance is $g_{md}$ (see Equation (4)) and the minimum supply voltage is zero (see Equation (5)). However, there is another condition given by (7) which limits the value of $\alpha$ in:

$$\alpha > -\frac{g_{md} + G_P}{g_{mg}} \tag{9}$$

Now, if we replace the value of $\alpha$ from Table 1 in (9), we obtain another condition for $L_g$:

$$L_g < \frac{1}{\omega^2 \left(C_{gs} + C_{gd} + \frac{C_{gd} g_{mg}}{g_{md} + G_P}\right)} \tag{10}$$

which prevails over (8) since $C_{gd}$, $g_{mg}$, $g_{md}$ and $G_P$ are all positive values. To sum up, the higher we choose $L_g$ within the range given by (10), the smaller is the supply voltage.

## 4. CIRCUIT DESIGN

The design starts with the choice of the aspect ratio and the DC characterization of the transistor. The best aspect ratio obtained was 200 $\mu$m/420 nm, which has a commitment between high transconductance and low parasitic capacitances. With a supply voltage of 40 mV the transistor parameters are: $C_{gs}$=103 fF, $C_{gd}$=102 fF, $g_{md}$=1.52 mS, $g_{mg}$= 2.50 mS and $g_{ms}$=4.50 mS. Choosing a value for $L_1$ in order to maximize $G_P$, we obtain $L_1$=9.18 nH and $G_P$=390 $\mu$S (considering that $G_P$ depends only on the $L_1$ parasitics, in first-order analysis). Using (10) the maximum value for $L_g$ is 13 nH. We chose $L_g$=12 nH which has a good quality factor in our frequency. Calculating (7), the optimum capacitor ratio is $K_{opt}$=1.08. From (6) and (3e), and for $f_o$ of 2.4 GHz, the value for the equivalent capacitance is $C_{eq}$=247 fF, thus $C_{1eq}$=476 fF and $C_{2eq}$=514 fF. Using (3c) and (3d) and the values for $Z_c$ and $Z_a$ from Table 1, the values for $C_1$ and $C_2$ are 541 fF and 704 fF, respectively. Note that $\omega(C_{1eq} + C_{2eq})$ is just 3.3 times $g_{ms}$, thus the optimum capacitor ratio is slightly different from the calculated by (7). The final $K_{opt}$ is 1.35.

## 5. SIMULATION RESULTS

It was developed a prototype in a standard 0.13 $\mu$m CMOS technology using a zero-$V_{TH}$ transistor. The results of the post-layout simulation are presented here. The final oscillator layout is shown in Figure 5. A buffer was designed in order to match the output of the oscillator with the 50 $\Omega$ impedance of the spectrum analyzer. The minimum sup-

**Table 2: Comparison between state-of-the-art CMOS oscillators**

| **Parameters** | [2] | [3]a | [3]b | [4] | This Work (simulated) |
|---|---|---|---|---|---|
| CMOS Technology (nm) | 130 | 180 | 180 | 180 | 130 |
| Supply Voltage (mV) | 475 | 600 | 400 | 350 | 40 |
| Frequency (GHz) | 4.90 | 5.60 | 5.60 | 1.40 | 2.12 |
| DC Power (mW) | 2.70 | 3.00 | 1.10 | 1.46 | 0.004 |
| Phase Noise (dBc/Hz) | -136.2 @ 3MHz | -118.0 @ 1MHz | -114.0 @ 1MHz | -128.6 @ 1MHz | -91.5 @ 1MHz |
| FoM* (dBc/Hz) | 196.3 | 189 | 189 | 189.8 | 182 |

*Figure of Merit = $20log\left(f_o/\Delta f\right) - 10log\left(P_{DC}/1mW\right) - L\left(\Delta f\right)$, $L\left(\Delta f\right)$ = phase-noise at $\Delta f$ offset frequency

ply voltage achieved by this circuit is 38 mV, but a better performance is achieved when the supply voltage is 40 mV.

Using (4) we obtain that the minimum source transconductance that allows the circuit start-up is 2.63 mS, which is smaller than the one supplied by the transistor, thus the circuit satisfies the start-up condition. The minimum supply voltage required to start-up oscillations from (5) is 18 mV, however, this is the start-up condition. Usually more energy is required to sustain oscillations.

When $Lg = 0$ the theoretical required start-up voltage would be 32 mV, about twice the required in our topology. The simulated minimum supply voltage achieved for this case was 70 mV, about twice the achieved with the new topology proposed here. The post-layout oscillation frequency was 2.12 GHz, which can be explained by the parasitic capacitances of the transistor which were not considered in the analysis, and layout parasitics.

Table 2 provides a comparison between some state-of-the-art oscillators in CMOS technology. As we can see, our prototype has a remarkable performance in power consumption and supply voltage. However the phase-noise is degraded, which depends directly on the output power, among other things. Nevertheless the circuit achieved a figure of merit comparable with other state-of-the-art CMOS oscillators.

## 6. CONCLUSION

In this paper we have presented a different topology for ultra-low voltage Colpitts Oscillator. By increasing the positive feedback, it was possible to decrease the required transconductance in order to start-up the oscillator, which causes a reduction in the supply voltage. The analysis was presented, as well as a step-by-step design and post-layout simulation results. According to the later, the use of the additional positive feedback allows to reduce the supply voltage as low as 40 mV, at a central frequency of 2.12 GHz, with a power consumption of 4 $\mu$W, phase-noise of -91.5 dBc/Hz @ 1 MHz, resulting in a figure of merit of 182 dBc/Hz.

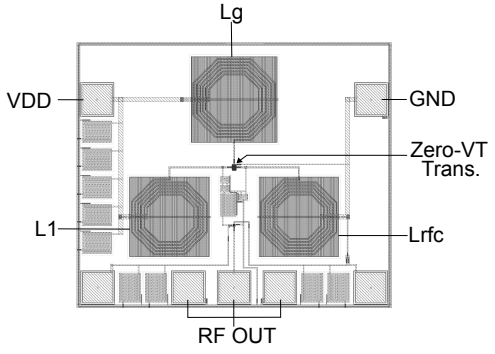


**Figure 5: Final oscillator layout.**

## 7. ACKNOWLEDGMENTS

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