Automatic OTA Miller Design by Optimization Procedure Using Simulated Annealing

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ABSTRACT
This paper presents the implementation of a tool for automatic synthesis of analog integrated basic blocks, using Simulated Annealing as main optimization heuristic and interface with an external electrical simulator. The methodology is based on the minimization of a cost function and a set of constraints in order to size each transistor of the circuit. As circuit design example, this paper shows the application of the methodology for the design of an OTA Miller in 0.18µm fabrication technology. For validation purposes, the results are compared with a manual typical analog design and with another result available in the literature. Results show that the circuit implemented with our tool presents better performance in terms of power consumption and gate area.

Keywords
Analog Design Automation, Simulated Annealing, CAD tool.

1. INTRODUCTION
Integrated circuits technology evolution is accelerated mainly by memory and microprocessor industries. Aggressive CMOS technology scaling generates digital circuits with more density of logical functions, increasing the memory capacity or the processing power. On the other hand, this evolution turns fabrication process more complex and with devices presenting more variability [1].

Analog circuits are present in most integrated circuits. Typical applications are signal processing and circuit interfaces between analog and digital domains. These circuits, although very sensible to process variations, must be compatible with standard digital fabrication technology, whose process variations increase as the size of devices decrease. Thus, the design of analog circuit is a great challenge in nanometer technologies.

Besides the design challenge, analog circuits lack from well-established design automation tools. Typical analog design is done manually by analog designers, with the aid of electrical simulators and layout editors. These characteristics result in an expensive design effort in terms of time and cost [2].

One characteristic that turns analog design a demanding task is the complex relationships between all design specifications (gain, bandwidth, power consumption, power supplies, etc.), allied to the large number of circuit free variables (transistors size, bias current, etc) [3]. With so many specifications, a competitive analog design becomes too complicated to be sized by manual calculations.

The analog design synthesis, in general, can be divided in three abstraction levels: system specification, circuit sizing and layout generation [4]. In the first level the circuit is seen as a black box and just the electrical behavior is relevant. In the circuit sizing level each individual device must be designed in order to obtain the electrical characteristics defined in the previous design stage. This task is, in general, performed using simplified equations that model the circuit and requires a high experience of the designer. In the layout level the IC layout is designed, based on the devices sizes. The interaction between the levels could be necessary if circuit characteristics are degraded during the synthesis processing.

In this context this paper proposes a tool to automatize a critical stage of analog circuit synthesis – the circuit sizing. The proposed tool is a simulated based tool with the sizing task based on an optimization procedure [10]. The design space is explored by artificial intelligence heuristics in order to find global solutions that satisfy the circuit constraints and optimize some goals of the circuit. As artificial intelligence heuristic we used the Simulated Annealing algorithm.

In order to evaluate the results, this paper presents a comparison of the design of an OTA Miller in XFAB 0.18µm technology implemented by a traditional manual design methodology and by using the proposed automatic tool. Also, the designed circuit is compared with another result available in the literature.

This work is organized as follows: section 2 shows the description of the proposed methodology; section 3 presents the results of the design of an OTA Miller circuit and section 4 shows the conclusion.

2. PROPOSED TOOL
The proposed methodology to automatic circuit sizing is based on modeling and solving an optimization problem. In this optimization problem the constraints (specifications whose values must be inside a given range) and design objectives (specifications to be optimized) are circuit specifications such as power consumption, silicon area, voltage gain, etc. The choice of which specification is a constraint or a design objective depends on the designer needs and is an option in the automatic tool. Constraints and goals are aggregated into a multi-objective cost function, which is used as a metric of circuit performance.

The general design flow is in according with [5] and is shown in Fig. 1. The inputs of the methodology flow are an initial solution for the circuit, design specifications (constraints and goals) and the fabrication technology parameters. Based in these inputs the optimization methodology provides values for the variables. For each generated solution the multi-objective cost function is calculated to evaluate the performance of the generated solution. The obtained performance is compared to the circuit specifications. The specification evaluation is obtained by electrical simulations with Synopsys HSPICE®.

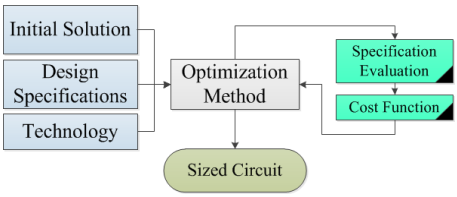

Figure 1 - Analog circuit sizing by an optimization method.

In this work we used the cost function shown in eq. (1). This equation is similar with the function used in [6]. The first sum represents the objective part the cost function and the second sum is the constraints part.

$$f_c = \sum_{i=1}^{n} P_{O_i}.S_i + \sum_{j=1}^{n} P_{R_j}.f(S_j) \quad (1)$$

S_i is the i^{th} specification of the circuit to be optimized and S_j is the j^{th} specification of the circuit that is constrained in a maximum or minimum value. P_{Oi} and P_{Rj} are values used as weighting purpose for normalization of specifications with different scales of magnitude. $f(S_j)$ is the cost function performance metric used to measure the distance between the required value to the specifications and the reached value. This function depends on the constraints type (minimum or maximum required value). These functions are shown in fig. 2.

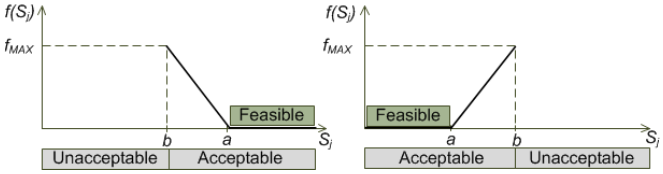

Figure 2 - Cost function performance metrics: (a) minimum required value specifications and (b) maximum required value specifications.

This work uses Simulated Annealing (SA) as the optimization algorithm. Simulated Annealing is a meta-heuristic for non-linear optimizations and it is inspired on the analogy of the thermodynamic principle of minimum energy state in the cooling of a heated set of atoms. This algorithm receives as input an initial solution and, at each iteration, it generates new solutions in a pseudo-random form. New solutions are generated by a generation function as the eq. 2. This equation depends on the current solution (X_c), a random normalized value (X_R) and the temperature parameter which decrease with the algorithm iterations by a function shown in Eq. 3.

$$X_N = X_C + \sqrt{T(i)}.X_R \quad (2)$$

$$T(i) = \frac{T_0}{\log(i)} \quad (3)$$

Each generated solution is compared with the current solution (X_c). If the cost function to the generated solution is better than previous, the generated becomes the actual solution. Otherwise, a random probability is evaluated and this solution becomes the current solution if the probability criterion is satisfied. This criterion is dependent on the temperature parameter so that the probability decreased with the iterations. This strategy is used for escaping from local minima.

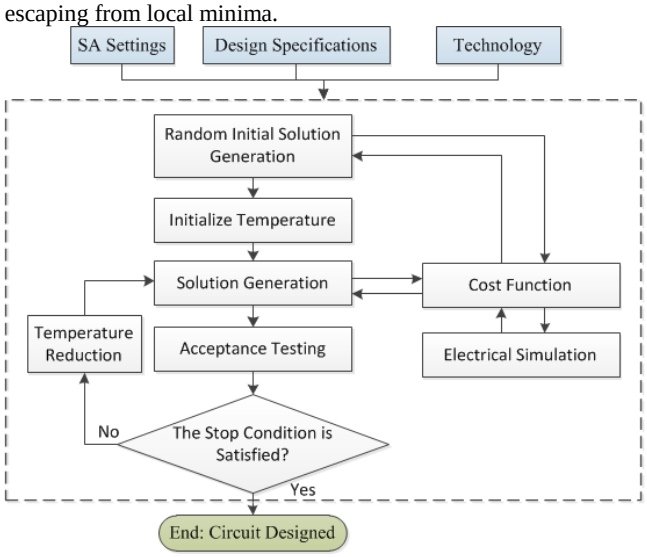

Figure 3 - Analog design flow with Simulated Annealing.

In this tool we used the implementation of Simulated Annealing algorithm provided by the Matlab Optimization Toolbox®.
With SA the methodology has the design flow shown in fig. 3. This flow has the design specifications, fabrication technology parameters and the SA setting as inputs. A random initial solution is generated and its performance is evaluated by cost function and electrical simulation. After the random initialization the initial temperature is set in the initial value. The generation function generates a new solution and the performance is evaluated by the cost function. Based on the solution performance and a random probability, the new solution can be accepted as current solution. The stop condition is tested and, if it is satisfied, the circuit is sized. If the stop condition is not satisfied, the temperature parameter is reduced and new solutions are generated. The stop condition to SA can be a minimum variation of a cost function, a minimum value of temperature, or other condition specified by the user.

3. OTA MILLER DESIGN

As design results, this work presents the design of a two-stage CMOS Miller operational transconductance amplifier (OTA).

The schematic of this amplifier is shown in fig. 4. The Miller OTA is composed by an input differential pair and a current mirror with active load in the first stage. The second stage is composed by an inverter amplifier. Between the first and second stages is connected a compensation capacitor (C_c) for stability purposes [7].
Main specifications for this circuit are low frequency gain (*Av0*), slew rate (*SR*), phase margin (*PM*), input common-mode range (*ICMR*), output swing (*OS*), power consumption and gate area.
For comparison, we performed two designs with different methodologies. First, a traditional manual design was implemented, using first-order model equations and a recipe-like methodology, such as the described by [7]. Next, the same circuit was sized with the proposed methodology using the automatic design tool.

For both designs we used the XFAB 0.18µm technology. In this technology the nominal voltage is 1.8V. The voltage sources VDD and VSS of the circuit are set to 0.9V e -0.9V, respectively. The load capacitance (C_L) and the compensation capacitor (C_c) are fixed in 3pF and 1pF, respectively.

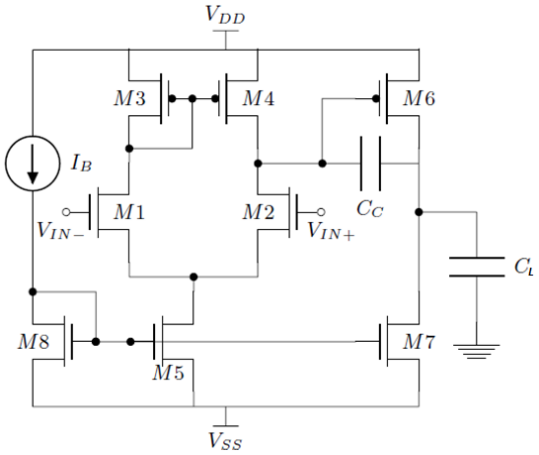

Figure 4 - Schematics of the two-stage CMOS Miller operational transconductance amplifier (OTA).

3.1 Manual Design

The manual design of an analog circuit requires large experience by the designer in circuit modeling, because the devices sizes are obtained by a design methodology that transcribe the design requirements into transistors sizes. Design methodologies can not be generalized and in general provide an initial solution to the circuit. An example of design methodology with simplified equations based on the SPICE MOS model Level 3 is presented in [7], taking as base the eq. 4 for the drain current in saturation. Another approach for modeling the circuit is proposed by [8], using the technology characteristic curve gm/ID as the base for transistor sizing. We adopt the methodology of [7] in this manual design of the OTA Miller of fig. 4. In this methodology the circuit is modeling by simplified equations in large and small signals. For example, the transistor aspect ratio of the transistor M1 (W1/L1) is based on the Eq. 5 that uses the *Av0* required specification and the simplified equations (6) and (7) to small signal approximation. In these equations g_{ds} is approximated by a linear variation λ (transistor channel length modulation parameter) that depends on the channel length (L).

$$I_D \cong \mu.C_{ox}.\frac{W}{L}.\frac{(V_{GS}-V_t)^2}{2} \quad (4)$$

$$Av0 \cong \frac{g_{m1}.g_{m6}}{(g_{ds2}+g_{ds4}).(g_{ds6}+g_{ds7})} \quad (5)$$

$$g_m \cong \sqrt{2.\mu_0.Cox.\frac{W}{L}|I_D|} \quad (6)$$

$$g_{ds} \cong \lambda.I_D \quad (7)$$

To design the circuit the specifications shown in the second column of tab. 1 are required. Using the approximated equations of [7] the initial transistor aspect ratio are obtained. With the initial transistors aspect ratio and electrical simulations the sizes W and L are obtained using an iterative analysis based on the required specifications. After a few iterations, the specifications shown in the third column of Tab. 1 are obtained. Transistor sizes are showed in Tab. 2.

Table 1. Specifications of OTA Miller design

Specifications	Required Value	Manual Design	Our work	Jafari et al. [11]
Av0 (dB)	≥ 70.00	78.98	82.62	82.4
GBW (MHz)	≥ 5.00	8.53	5.23	9.77
PM (°)	≥ 60.00	60	61	60
SR (V/µs)	≥ 5.00	8.54	6.38	5.07
ICMR+ (V)	≥ 0.70	0.80	0.84	-
ICMR- (V)	≤ -0.70	-0.71	-0.72	-
Output Swing (V)	≥ 1.00	1.15	1.18	1.17
Pdiss (µW)	Minimize	77.08	12.91	52.00
Gate Area (µm²)	Minimize	34.86	16.88	236.25

Table 2. Parameter of OTA Miller design

Specifications	Manual Design	Our work
W1/L1(µm/ µm) Inversion Level	1.27/0.4 Moderate	2.88/0.27 Weak
W3/L3(µm/ µm) Inversion Level	2.97/0.27 Moderate	5.84/0.21 Weak
W5/L5(µm/ µm) Inversion Level	1.6/0.4 Strong	1.42/0.90 Moderate
W6/L6(µm/ µm) Inversion Level	48.8/0.44 Moderate	31.90/0.26 Weak
W7/L7(µm/ µm) Inversion Level	10.8/0.9 Moderate	2.36/0.82 Moderate
I_{BIAS}(µA)	10.3	2.01

3.2 Automatic Design

For the automatic design procedure, the developed tool was configured to optimize the cost function with the required specifications of tab. 1. The goal of the design is to minimize the power dissipation and the gate area.

Based on the XFAB 0.18µm technology, the variable bounds of the optimization are set to 0.18µm≤L≤20µm, 0.22µm≤W≤100µm and 1µA≤IB≤100µA. SA was configured to use Boltzmann functions of [9] for solution generation and temperature evolution.

The cost function is according to following equation:

$$f_c = \frac{1}{70\times10^{-6}}.Power + \frac{1}{30\times10^{-6}}.Area + \sum_{j=1}^{n} P_{R_j}.f(S_j) \quad (8)$$

In this equation the optimization weighting values are set in reference to the manual design shown in Tab.1. To the specifications, P_{Rj} are set equal to the unity.

The tool was executed and the results of the automatic synthesis are shown in the fourth column of tab. 1. The variables values of the obtained solution are shown in tab.2.

To compare these results with another automatic sizing tool the fifth column of Tab. 1 shows the results reached by Jafari et al. [11] to the same circuit. The tool proposed in [11] is based on a design process with simplified equations using genetic algorithms. To validate the solutions, electrical simulations are performed at the end of design procedure.

The results of Tab.1 shows that the better result is obtained with the automatic methodology proposed in this work. The comparison shows that all required values of the specifications are reached. With the automated design procedure we found a

solution that is about 83.25% and 51.58% better than the manual design in terms of gate area and power dissipation, respectively. A comparison with [11] shows that our automation procedure is about 92.86% and 75.17% better for the same specifications.

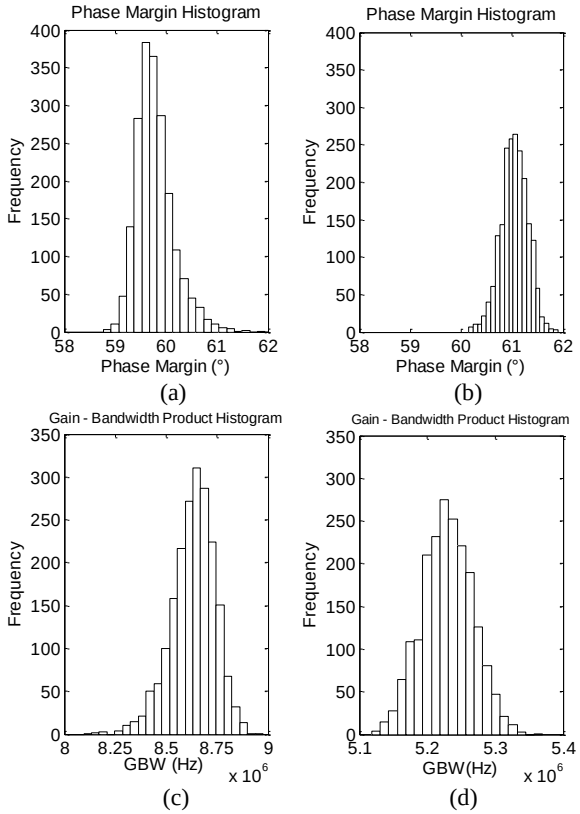

Figure 5 - Frequency histogram for the Monte Carlo simulation of Phase Margin for manual (a) and automatic (b) designs and Gain-Bandwidth Product for the manual (c) and automatic (d) designs.

Our proposed design procedure presented better results due the fact that it is capable to explore efficiently the entire design space, including weak and inversion regions of transistors. The same does not happen in the manual design and in the methodology proposed in [11]. Low power solutions are in general obtained in weak and moderated inversion, regions that are better explored by electrical simulations.

An important analysis of the analog design is the circuit electrical behavior under some process parameter variation. To analyze the effect of parameter variation, Monte Carlo simulation is performed over 2000 evaluations. To the results shown, the calculated yield of the solution generated by the automatic procedure is about 90% and in the manual design is about 65%. Analyzing the results of tab. 1 it is possible to see that, in general, the reached specifications are much larger than the required values. Thus, even with variations the specifications are in according to the required values. However, the reached solutions that are next to the required values can be more affected by the variations and reduce the yield of the solution. This result is seen in fig. 5. To the Phase Margin (parts a and b of fig. 5), which is close to the required value, the histogram has some values below the required value. In the parts (c) and (d) of this figure we can see that the gain–bandwidth product (GBW) is not below the required values because this value is much larger than the required value.

4. CONCLUSION

This work proposes a tool for the automatic design of an OTA Miller circuit using Simulated Annealing optimization heuristic. The design in technology XFAB 0.18µm was performed in manual and automated form. Results show that the proposed tool presents better design solutions than the manual design. Also, comparing with other solutions in the literature, our tool obtained again better results. One of the causes of these results is that in our proposed tool the entire design space is explored, including weak and moderate inversion levels.

As future work, we intent to compare the tool with other circuit topologies and optimization heuristics. We intend to insert an analysis of parameter variation using some design centering optimization methodology.

5. ACKNOWLEDGMENTS

The grant provided by CNPq Brazilian research agency for supporting this work is gratefully acknowledged.

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