Characterization of CMOS Fully Differential Amplifiers for Automatic Design Procedure

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ABSTRACT
This paper presents the design and characterization of fully differential amplifiers for application in an automatic circuit sizing tool. The tool uses Simulated Annealing as main optimization heuristic and electrical simulations for circuit specifications evaluations. The methodology is based on the minimization of a cost function and a set of constraints in order to size each transistor of the circuit. A set of standard testbenches are implemented in the tool to estimate the specifications values. In these testbenches an ideal common-mode feedback (CMFB) circuit is used. As design example, this paper shows the application of the approach for the design of a single-stage fully differential amplifier in 0.18 μm technology. The results show that all required specifications are met in an acceptable execution time.

Categories and Subject Descriptors
B.7 [**INTEGRATED CIRCUITS**]: Design Aids—*automatic synthesis, simulation, optimization*

General Terms
Algorithms, Measurement, Design

Keywords
Analog Design Automation, Characterization, CAD tool

1. INTRODUCTION
Differential signaling has been commonly used in audio, data transmission, and telephone systems for many years because of its inherent resistance to external noise sources. Today, differential signaling is becoming popular in high-speed data acquisition, where the inputs of analog-to-digital converters are differential [5].

Thereby, the fully differential amplifiers are indispensable in the implementation of circuits that use differential signaling. Fully differential op amps are widely used in modern integrated circuits because they have some advantages over their single-ended counterparts. They provide a larger output voltage swing and are less susceptible to common-mode noise. Also, even-order non-linearities are not present in the differential output of a balanced circuit [3]. On the other hand, fully differential amplifiers need two feedback networks and a common-mode feedback(CMFB) circuit to control the common-mode voltage at output [3] [4].

As there are multiple methods to do such task, to design such feedback circuit we need to consider parameters that have direct influence on the specifications of the main fully differential amplifier. In this context, the methodology described in this paper proposes the implementation of fully differential amplifiers in an automatic circuit sizing tool based on modeling and solving an optimization problem. The design of the op-amp is made using a ideal common-mode feedback circuit, allowing the tool to size only the differential part of the amplifier without care with the CMFB circuit.

As results, this papers presents a single-stage amplifier in 0.18 μm technology using the UCAF automatic sizing tool [8] with the presented testbenches.

The rest of this paper is organized as follows: section 2 shows the description of the UCAF automatic sizing tool; section 3 presents the testbenches for circuit characterization and the CMFB block; section 4 shows the results of the automatic single-stage fully differential amplifier design; and section 5 presents the conclusions.

2. UCAF: ANALOG INTEGRATED CIRCUIT SIZING TOOL
The implementation of this work is based on the UCAF tool. This tool was implemented in Matlab® and uses artificial intelligence to explore the design space in order to find optimized solutions. These solutions should satisfy some design constraints and to optimize some design specifications, such as power dissipation and silicon area. The design methodology of the UCAF tool is based on the design flow shown in Figure 1. The inputs of the tool are the initial solution for the circuit, design specifications (constraints and goals) and the fabrication technology parameters. Based on these inputs, the optimization algorithm (like simulated annealing), provides values for the circuit variables. These values are possible solutions for the circuit. The variables in the sizing process are the transistors channel length (L) and width (W) and the voltages or currents source bias. Each possible solution is evaluated based on the circuit specifications. Based on this evaluation the optimization method exploits the design space to find optimized solutions.

In the UCAF tool the optimization procedure has a cost function according to eq. (1). In this equation, E_i is the specification that must be optimized. There can be n specifications according to designer needs. In this paper we used the minimization of power dissipation and gate area as design goals. $f(E_j)$ is the performance metric dependent on the specifications that are constrained in minimum or maximum values. The representation of this function is shown in Figure 2 and is dependent on the type of specification (minimum,

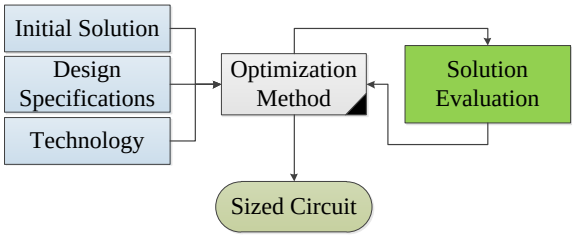
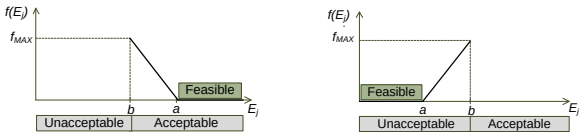


Figure 1: The design methodology implemented in the UCAF tool.



(a) (b)

Figure 2: Cost function performance metric, (a) minimum required value specifications and (b) maximum required value specifications.

as depicted in Figure 2(a), or maximum, as depicted in Figure 2(b)) and on the bounds of feasible and acceptable solutions a and b, respectively [2]. P_{O_i} and P_{R_i} are the weight parameters for each specification.

$$f_c = \sum_{i=1}^{n} P_{O_i}.E_i + \sum_{j=1}^{n} P_{R_j}.f(E_j) \quad (1)$$

An important characteristic of this cost function is that non feasible solutions are admitted as a possible circuit solution. As shown in Figure 2, unfeasible solutions have $f(E_j)$ values that depend on the distance between a required value and the measured specification value (E_j). It is important because a worst solution can be a path to a good solution in the design space exploration. If these solutions are ignored the algorithm can not explore this region effectively [6].

This work uses Simulated Annealing (SA) as the optimization algorithm. Simulated Annealing is a meta-heuristic for non-linear optimizations and it is inspired on the analogy of the thermodynamic principle of minimum energy state in the cooling of a heated set of atoms. With SA the methodology has the design flow shown in Figure 3. This flow has the design specifications, fabrication technology parameters and the SA setting as inputs. A random initial solution is generated and its performance is evaluated by cost function and electrical simulation. After the random initialization the initial temperature is set in the initial value. The generation function generates a new solution and the performance is evaluated by the cost function. Based on the solution performance and a random probability, the new solution can be accepted as current solution. The stop condition is tested and, if it is satisfied, the circuit is sized. If the stop condition is not satisfied, the temperature parameter is reduced and new solutions are generated. The stop condition to SA can be a minimum variation of a cost function, a minimum value of temperature or other condition specified by the user [9].

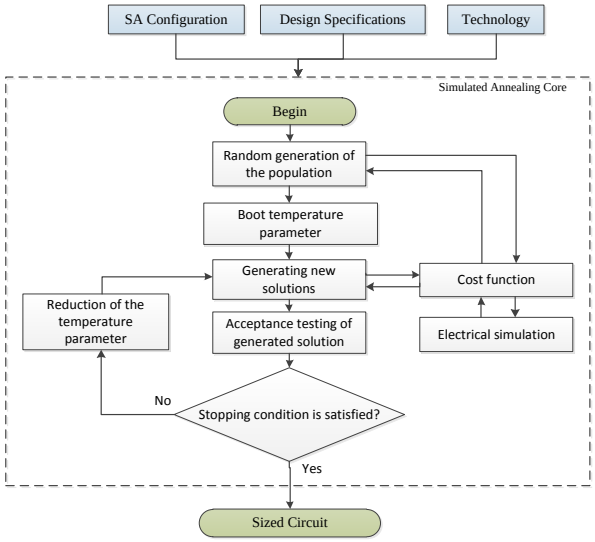


Figure 3: Analog design flow with Simulated Annealing.

3. FULLY-DIFFERENTIAL AMPLIFIER CHARACTERIZATION

This section presents the standard testbenches and the ideal CMFB circuit implemented in the UCAF automatic sizing tool. These testbenches are based on [1][3][4].

3.1 Implemented Testbenches

The automatic sizing tool uses several circuits testbenches to estimate the circuit specifications. These estimations are obtained with the electrical simulation. Figure 3.1 shows the testbenches that are implemented in the tool. An AC analysis is performed to measure low-frequency gain (A_{v0}), gain-bandwidth product (GBW) and phase margin (PM). The configuration used for this measure is shown in the Figure 4(c) [7]. The results of this simulation can be plotted as a Bode diagram. From the gain curve of this diagram, A_{v0} and GBW specifications are extracted. In the same way, the phase margin is obtained in the phase curve for a frequency equal to the GBW, as shown in Figure 5.

To obtain some circuit specifications as slew rate (SR) and Input Common Mode Range (ICMR), a unitary gain configuration is needed. The circuits of fig. 4(a) and 4(b) are used to obtain this configuration . In these circuits the voltage gain is equal to

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_f}{R_g} \quad (2)$$

Then, for a unitary gain, the resistors R_f and R_g are set to be equal, where $R_f = R_g = 10\ k\Omega$.

To measure the response speed of an amplifier (slew rate), a pulse voltage is applied in the unitary gain configuration (Figure 4(a)). However, the goal of this simulation is the analysis of the step response of the circuit through the verification of the output voltage level in a transient analysis [7]. The SR value represent the velocity to drive a capacitive load.

To obtain the Input Common Mode Range (ICMR), a variable DC supply is connected in the unity gain configuration, as shown in

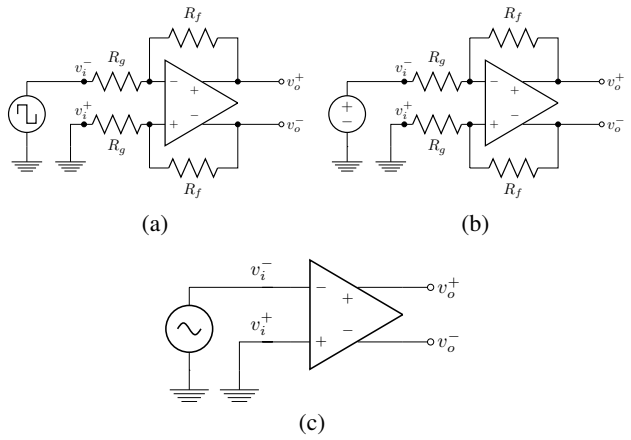


Figure 4: Implemented testbenches for the fully differential amplifier, (a) Slew Rate, (b) ICMR and (c) AC open loop.

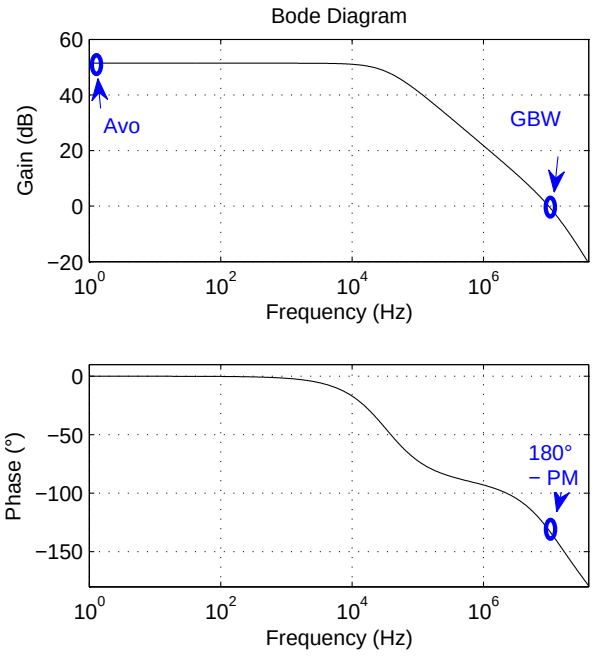


Figure 5: Bode diagram used to estimate low-frequency gain (A_{v0}), gain-bandwidth product (GBW) and phase margin (PM).

Figure 4(b). In this simulation, the input voltage is varied from a minimum to a maximum level in a DC analysis. Positive and negative values are obtained from simulation output when the gain is linear [7]. This specification represents the minimum and maximum common mode of the input signal.

3.2 Common-Mode Feedback

The main problem of the design of fully differential amplifiers is the common-mode feedback (CMFB). The CMFB circuit is a feedback circuit used to keep the average of the outputs (the common-mode output voltage) equal to a reference value. However, this circuit need to compare the common-mode output voltage with the

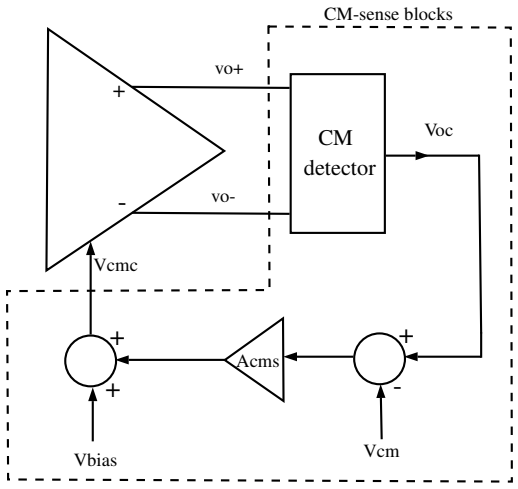


Figure 6: A conceptual block diagram of the CMFB [3].

reference value. Based on this difference, the reference current of the fully differential amplifier is increased or decreased. Several control strategies can be used as CMFB circuit. Figure 6 presents a CMFB scheme.

The CM-sense block is composed by a CM detector, which calculates the average of the amplifier outputs: $V_{oc} = \frac{V_{O+}+V_{O-}}{2}$. This voltage is subtracted from the desired CM output voltage, V_{cm}. The difference between the CM output voltage and its desired value, $V_{oc} - V_{cm}$, is amplified by a gain A_{cms}. The resulting value is then added with the DC bias voltage V_{bias}. The result is V_{cmc}, where

$$V_{cmc} = A_{cms}(V_{oc} - V_{cm}) + V_{bias} \quad (3)$$

The CMC (common-mode control) input is chosen so that changing V_{cmc} changes V_{oc} but does not affect V_{od} (differential output voltage) if the circuit is perfectly balanced [3]. In this work, an ideal circuit which implements the eq. 3 is used together with the implemented testbenches of the previous subsection.

4. DESIGN RESULTS

As an example of the proposed approach, the design of a single-stage CMOS fully differential amplifier in 0.18 μm technology with nominal voltage of 1.8 V is presented. The circuit schematic is shown in Figure 7. The voltage sources V_{DD} and V_{SS} of the circuit are set to 0.9 V and -0.9 V, respectively. Both load capacitances (C_L) are fixed in $10pF$. For this amplifier, the CMC input node is the gate of M5. If the gain in the CMFB loop is high, the negative feedback forces $V_{oc} \approx V_{cm}$ and V_{cmc} to be approximately constant with $V_{cmc} \approx V_{bias}$. Transistor M5 supplies the tail current for the pair M1 and M2. Bias voltage V_{bias} is added to provide the nominal DC component of V_{cmc} that sets $I_5 = |I_3|+|I_4|$ when $V_{oc} = V_{cm}$ [3]. The ideal CMFB has influence only in the gate voltage of M5, V_{B1}, such that $V_{cmc} = V_{B1}$.

For the optimization process, the design has transistor sizes and the bias voltage as free variables. So this design has the following 8 free variables: W_1, L_1, W_3, L_3, W_5, L_5, V_{B1} and V_{B2}. The optimization procedure uses the Simulated Annealing algorithm as optimization heuristic. The main specifications for this circuit are

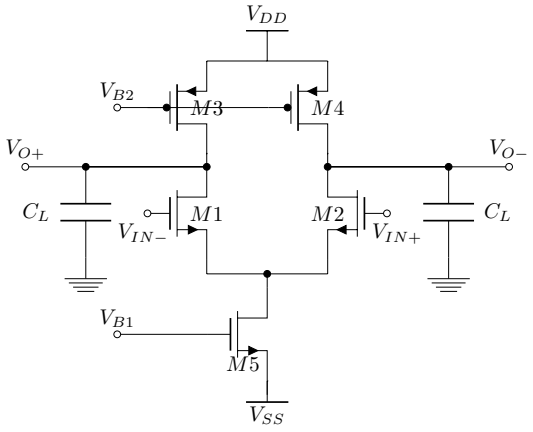


Figure 7: Schematics of a single-stage fully-differential CMOS amplifier.

low frequency gain (A_{v0}), slew rate (SR), phase margin (PM) and input common-mode range ($ICMR$). The required and obtained values for the automatic design is shown in Table 1. Power dissipation is set as design objective and the other specifications are maintained as design constraints. The obtained transistor sizes for the amplifier are presented in Table 2.

The results show that all constraints are met and the power dissipation for the circuit is optimized to $4.891\ \mu W$. The execution time is less than 2 hours.

5. CONCLUSIONS

The proposed approach for the design and characterization of fully differential amplifiers presented good results when included in an automatic sizing tool. The implementation doesn't consider the CMFB circuit to sizing the main amplifier, which gives to the designer the freedom to choose separately the topology of the CMFB circuit. As the results show that the amplifier have a proper operation with the ideal CMFB, in future work we intent to design the CMFB circuit based on the data obtained by the design with the ideal circuit. The output voltage of the CMFB must float around the nominal common-mode control voltage.

Table 1: Results obtained for the single-stage fully differential amplifier.

Specifications	Required Value	Obtained Value
A_{v0} (dB)	$\geq$ 30.00	31.535
GBW (MHz)	$\geq$ 1.00	1.023
PM (^{o})	$\geq$ 50.00	91.46
SR (V/μs)	$\geq$ 1.50	4.217
ICMR+ (V)	$\geq$ 0.40	0.51
ICMR- (V)	≤ -0.40	-0.888
P_{diss} (μW)	Minimize	4.892
Run Time (min)	-	118

Table 2: Obtained transistor sizes for the designed amplifier.

Specifications	Obtained Value
W_1/L_1 (μm/μm)	40.77/9.07
W_3/L_3 (μm/μm)	6.54/9.14
W_5/L_5 (μm/μm)	31.69/1.13
V_{B1} (mV)	250.64
V_{B2} (mV)	-384.78

6. ACKNOWLEDGMENTS

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7. REFERENCES

[1] P. E. Allen and D. R. Holberg. *CMOS Analog Circuit Design*. Oxford University Press, 2nd edition, 2002.

[2] S. Deyati and P. Mandal. An automated design methodology for yield aware analog circuit synthesis in submicron technology. In *Quality Electronic Design (ISQED), 2011 12th International Symposium on*, pages 1–7, 2011.

[3] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer. *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 2001.

[4] R. Gregorian and G. Temes. *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley, 1986.

[5] J. Karki. Fully-differential amplifiers, analog application report. Technical report, Texas Instruments, 2001.

[6] B. Liu, F. Fernandez, and G. G. E. Gielen. Efficient and accurate statistical analog yield optimization and variation-aware circuit sizing based on computational intelligence techniques. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 30(6):793–805, 2011.

[7] A. C. Oliveira, L. Severo, and A. Girardi. Parallel characterization of operational amplifiers for acceleration of design optimization. *South Symposium on Microelectronics - SIM*, Porto Alegre-RS. SIM 2013.

[8] L. Severo and A. Girardi. Ucaf a framework for analog integrated circuit analysis and design. *XI Microelectronics Students Forum (SForum 2011) - Chip on the Cliffs*, 2011.

[9] L. Severo, D. Longaretti, and A. Girardi. Automatic ota miller design by optimization procedure using simulated annealing. *XII Microelectronics Students Forum - SForum*, 2012.

[10] L. C. Severo, A. Girardi, A. B. de Oliveira, F. N. Kepler, and M. C. Cera. *Simulated Annealing to Improve Analog Integrated Circuit Design: Trade-Offs and Implementation Issues, Simulated Annealing - Single and Multiple Objective Problems, Dr. Marcos Sales Guerra Tsuzuki (Ed.),*. InTech, 2012.