

Hamming and Hopfield single-electron neural networks: a performance comparison

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ABSTRACT

The goal of this work is to compare two architectures of single-electron neural networks performing a pattern recognition task. Comparison was made regarding 6 very important characteristics of circuits: power dissipation, occupied area, bandwidth, response delay, stability plot and robustness to noise. All the simulations were made at room temperature (300 K) and at 0 K. Power dissipation and occupied area were calculated by well known mathematical formulas, bandwidth and response delay were estimated using SECS (Single-Electron Circuit Simulator) and stability plot and robustness to noise were achieved by using SIMON (Simulation of Nano-structures). The Hamming network presented the best performance. Nevertheless, the Hopfield network can be advantageous in some particular aspects.

Keywords

Single-electron neural networks, nanoelectronics, pattern recognition.

1. INTRODUCTION

The electronic industry finds itself at the verge of a revolution: economic pressure requires faster and smaller devices capable of high processing speed and low power consumption. These requirements have been, until now, met by the MOSFET (Metal Oxide Semiconductor Field Effect Transistor). The drawback of this device are its dimensions: they are still micrometric. As scientists advance in the search for more efficient devices, something becomes clear: nanoelectronics is the next logical step in the progress of electronic industry [8][10]. In this context, several new devices have been proposed, such as resonant tunneling diodes (RTD), quantum dots (QD) and single-electron tunneling transistors (SET) [8]. A SET is capable of confining electrons to very small dimensions so that the quantization of its charge and its energy are easily observed [11]. In this way, SETs are essentially quantum devices. There are many proposals of new circuits implemented in SET technology. Among

these circuits some neural networks architectures have been proposed [3, 6, 7].

Artificial neural networks can be implemented by electronic circuits that are capable of performing activities of high complexity [2]. Taking that into account two architectures of nanoelectronic neural networks based on SETs were chosen for a performance comparison in a pattern recognition task: Hamming network [3] and Hopfield network [6], both were proposed in former works. The performance of these circuits was simulated using two softwares: SIMON [11] and SECS [12]. The main difference between these two simulators is the fact that SECS allows frequency simulations by introducing a time scale into simulation. This time scale is based on the occurrence of a tunneling event, i.e., the time scale is increased every time a tunneling event occurs. Although both simulators use the Monte Carlo method to incorporate the stochastic nature of tunneling events, there are some differences in the simulation process beyond the time scale [12]. One of these differences is of great significance in this work: the fact that SECS does not include the occurrence of rare events in its simulation. So, one might say that there is an inherent comparison here: the comparison between two nanoelectronic circuits simulators.

2. CIRCUITS AND SIMULATIONS

In order to make a fair comparison, the same patterns (shown in the first column of table 1) were presented as inputs to both networks. To do that, each pattern was converted into a vector with 9 elements (3 for each line of the image). For example let's take the first pattern presented in the second column of table 1: the first line is represented by the vector (1, 0, 1), the second by (0, 1, 0) and the third by (1, 0, 1). The result is the vector (1, 0, 1, 0, 1, 0, 1, 0, 1), where 1 stands for a black square and 0 for a white one [3]. In the second column of table 1 the three patterns used to train the networks are presented as desired outputs corresponding to each input. To train these patterns, Hopfield network needs 9 inputs and 9 outputs. This happens because Hopfield network has one output for each little square that composes the pattern. Hamming network needs 9 inputs and only 3 outputs, due to its Winner-Take-All (WTA) layer, which associates each pattern to only one output [3].

The artificial neural networks used in this work were designed according to the methods developed by Guimarães et al. [3] and by Peixoto et al. [7]. The resulting circuits are shown in figures 1 and 2.

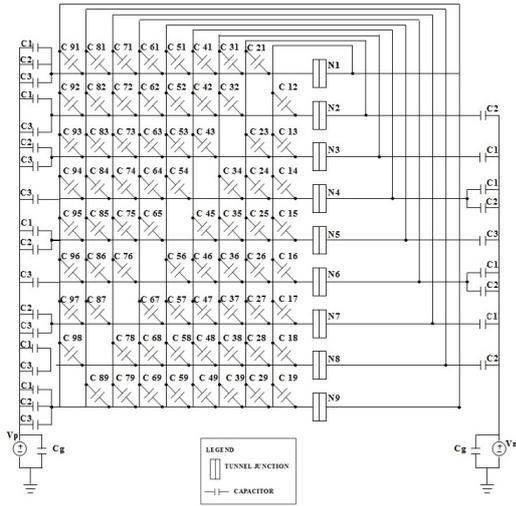


Figure 1: Hopfield network (modified [7]).

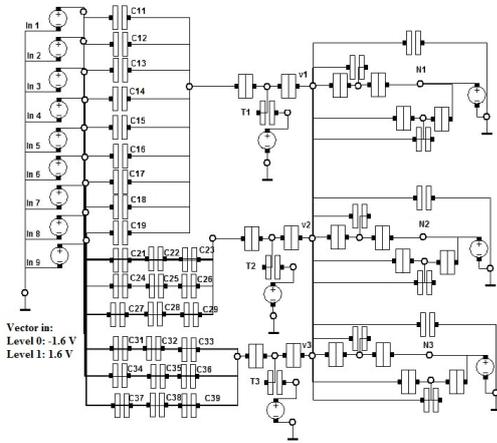


Figure 2: Hamming network designed in SIMON.

Table 1: Patterns presented to the networks

Presented pattern - in	Expected pattern - out

The estimations of occupied area were calculated using the following data: each $5\mu\text{F}$ capacitance occupies 1cm^2 [5][1] and a tunnel junction area is of $70\text{fF}/\mu\text{m}^2$ [9]. The power dissipation estimation is divided into two parts: static power (P_{stc}) and dynamic power (P_d) [4].

$$P_{stc} = V_{DD} \cdot I_{lkg}, \quad (1)$$

$$P_d = C_L \cdot V_{DD}^2 \cdot f, \quad (2)$$

where, V_{DD} is bias voltage, I_{lkg} is the leakage current measured in the output of the transistors of the input layer (Hamming network) or in the output of the tunnel junctions (Hopfield network), C_L is the total capacitance connected to the output node and f is the operating frequency. Here, f is equal to 1 GHz.

In order for estimating bandwidth and response delay the circuits were simulated in SECS. The bandwidth was obtained by simply increasing the operating frequency of the circuit up to the maximum point where the correct outputs are still provided by the network. The response delay were calculated as the difference between the time when the input signal reaches 50% of its final value and the time when the latest output reaches 50% of its final value. Because the circuits have more than one output (Hamming network has 3 outputs and Hopfield has 9), the latest output was chosen, so the worst case could be simulated.

Stability plot and robustness to noise were simulated using SIMON. In order to evaluate the stability of both networks at room temperature, their stability plot was obtained. At each point of the stability plot, the free energy of the circuits is calculated based on the variation of the input voltages applied to the circuit. The higher the free energy of the circuit, the greater the probability of occurring charge oscillations. In this way the stability plot displays regions where stable and unstable points can be identified by the change of color: stable points are colored white whereas unstable points are colored black. The rest of the points are colored grey - the darker the region, the more unstable it is. For Hopfield network the operation point is determined by the value of the source connected to its inputs, V_{in} , and by the value of the source connected to its outputs V_{out} (shown in figure 1 as V_p and V_n , respectively). In this case, since there is only one value of $V_p = V_{out} = V_n = V_{in}$, the point of operation will be $(V_{in}, V_{in}) = (-70\text{V}, -70\text{V})$, the reason for this sources to be equal can be seen in [7]. For Hamming network, as shown in figure 2, there are two values for the source connected to the input layer, V_{in} : 1,6 V and -1,6 V, for levels 1 and 0. There is also another source called V_{bias} that is connected to each SET of the WTA layer [3]. In this way, Hamming network needs two stability plots: V_{in} versus V_{in} and V_{bias} versus V_{in} , the first one will result an area and the second one a line.

Robustness to noise were obtained by introducing random charges in the circuits. These random charges are multiples of the elementary charge e . The amount of random charges were increased until the circuit's operation were uncharac-

teristic.

3. RESULTS

Table 2 shows the occupied area for each network at room temperature and at 0 K.

Table 2: Total area occupied by Hopfield and Hamming networks at 0 and at 300 K.

Network	Total area at 0 K	Total area at 300 K
Hopfield	286,1286 μm^2	2,989 ηm^2
Hamming	6,51 μm^2	71,769 ηm^2

It can be seen that Hamming network occupies a smaller area at 0 K, the reason for that is the fact that Hamming network has fewer capacitors and tunnel junctions than Hopfield network. Hopfield network has better results concerning occupied area at 300 K, as for operating in higher temperatures the capacitances should be smaller. In Hopfield network, this reduction is about two orders of magnitude greater than in Hamming network and a smaller capacitance occupies less area.

Table 3 shows the results obtained for power dissipation for Hopfield network and table 4 for Hamming network.

Table 3: Power dissipated by Hopfield network at 0 and at 300 K

Power	0 K	300 K
Static	0 W	10,0937466 fW
Dynamic	-	-
Total ($P_{stc} + P_d$)	0 W	10,0937466 fW

Table 4: Power dissipated by Hamming network at 0 and at 300 K

Power	Hamming (0 K)	Hamming (300 K)
Static	0 W	17,088 pW
Dynamic	768 ηW	3,072 μW
Total ($P_{stc} + P_d$)	768 ηW	3,072 μW

Unfortunately, Hopfield network could not be simulated in SECS and the reason for that is quite simple: SECS does not include rare events in its simulation process. This means that there are no simulation of cotunneling events and, as can be seen in [6], cotunneling events are essential to quantum Hopfield network operation. Because of that, the comparison regarding bandwidth and response delay could not be made and the power dissipation of Hopfield network is represented only by the static value, since the dynamic value depends directly on the frequency. The comparison regarding power dissipation can be made taking into consideration

only the static power. In this case, at 300 K, Hamming network dissipates a power 1,692.9 times greater than Hopfield network.

The bandwidth and the delay response simulations were performed only in the Hamming network, since the behavior of Hopfield network was not validated in SECS. For the first simulation it was observed that Hamming network can operate in frequencies up to 15 GHz, depending on the time delay that the application can tolerate (for higher frequencies the response delay is greater). Table 5 shows the results obtain for Hamming network at room temperature.

Table 5: Response delay for Hamming network at 300 K.

Frequency	Period (T)	Delay (t_d)	% of T
1 GHz	1 ηs	62,8 ps	6,28 %
2 GHz	0,5 ηs	50,11 ps	10,02 %
5 GHz	0,2 ηs	42,22 ps	21,11 %
10 GHz	0,1 ηs	13,74 ps	13,74 %
15 GHz	0,067 ηs	17,92 ps	26,88 %

A stability plot will show the operation point of the circuit: if it stays in a white area, the operation is stable. Figure 3 shows the results for the networks at each operation point.

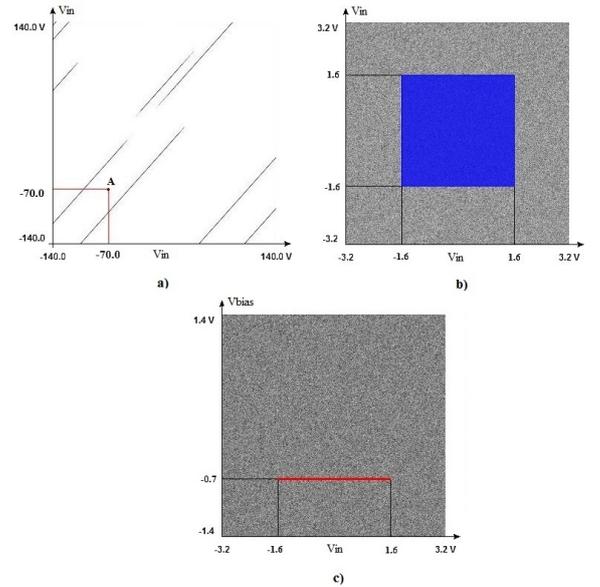


Figure 3: All plots at 300 K. a) Hopfield stability plot. b) Hamming stability plot - V_{in} versus V_{in} . c) Hamming stability plot - V_{bias} versus V_{in} .

The robustness to noise for each network is presented next. To obtain the results shown in table 6, the third pattern of the second column of table 1 was presented to the network. It can be noted that Hopfield network does not tolerate noise. That was already expected, since this network needs to know accurately the amount of charge of each node

to operate correctly. In other works, it needs to know if the electron is or is not in the node.

Table 6: Robustness to noise of $0,1 \cdot e$ - Hopfield network at 300 K.

Neuron	Expected Charge [C]	Obtained Charge [C]
1	e	$0.00625 \cdot e$
2	e	$0.00625 \cdot e$
3	e	$0.005 \cdot e$
4	e	$0.003125 \cdot e$
5	0	$0.004375 \cdot e$
6	e	$0.00375 \cdot e$
7	e	$0.00125 \cdot e$
8	e	$0.00625 \cdot e$
9	e	$0.00625 \cdot e$

The result for Hamming network was much better: it can operate with noise up to 45% of e .

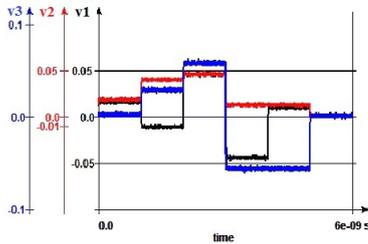


Figure 4: Hamming network at 300 K: well characterized operation with noise of 45% of e .

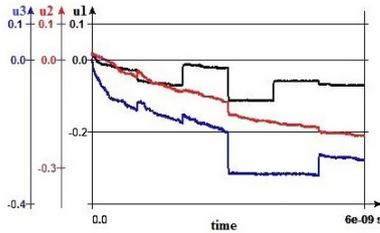


Figure 5: Hamming network at 300 K: loss of functionality with noise of 46% of e .

4. CONCLUSIONS

The goal of this work was to compare two architectures of nanoelectronics neural networks (Hamming and Hopfield). Both of the circuits have already been validated in SIMON. Thus, one of the challenges was to validate the networks behavior in the new single-electron circuit simulator SECS. As was shown, Hopfield network could not be simulated in SECS. Regarding the comparison parameters, Hopfield network was better concerning occupied area at room temperature, static power dissipation and stability plot. With respect to more qualitative aspects, Hamming network is easier to work with. The desingning is simpler and the circuit is smaller.

5. REFERENCES

- [1] A. Ali, H. Madan, R. Misra, A. Agrawal, P. Schiffer, J. B. Boos, B. R. Bennett, and S. Datto. Experimental determination of quantum and centros capacitance in arsenide-antimonide. *IEEE Transactions on Electron Devices*, 58(5), 2011.
- [2] L. Fausett. *Fundamentals of Neural Networks*. Prentice-Hall, New Jersey USA, 1994.
- [3] J. Guimarães, L. Nobrega, and J. da Costa. Design of a hamming neural network based on single-electron tunneling devices. *Microelectronics Journal, Holland*, 37(6):510–518, 2006.
- [4] L. B. H. J. Moon-Young and J. Yoon-Ha. Design considerations for low power single electron transistor logic circuits. *Japanese Journal of Applied Physics*, 40, 2001.
- [5] P. S. K. Karre and P. L. Bergstrom. Room temperature operational single electron transistor fabricated by focused ion beam deposition. *Journal of Applied Physics*, 102, 2007.
- [6] N. A. e. Y. A. Masamichi Akazawa, Eriko Tokuda. Quantum hopfield network using single-electron circuits - a novel hopfield network free from local-minimum difficulty. *Analog Integrated Circuits and Signal Processing*, 24:51–57, 2000.
- [7] C. P. S. M. Nogueira and J. G. Guimarães. Pattern recognition based on auto-associative single-electron neural network. *J. Comput. Theor. Nanosci*, 9:974–979, 2012.
- [8] D. J. Paul. Nanoelectronics. *Encyclopedia of physical science and technology*, 10:285 – 301, 2002.
- [9] M. M. T. Holmqvist and J. P. Pekola. Double oxidation scheme for tunnel junction fabrication. *J. Vac. Sci. Technol.*, 26:28–31, 2008.
- [10] G. Tegart. Nanotechnology: The technology for the 21st century. *The second international conference on Technology foresight*, 2003.
- [11] C. Wasshuber. Single-electronics - how it works. how it's used. how it's simulated. In *IEEE Computer Society*, 2002.
- [12] G. T. Zardalidis and I. Karafyllidis. Secs: A new single-electron-circuit simulator. *IEEE Trans. on Circuits and Systems*, 55-I(9):2774–2784, 2008.