Design of a CMOS 921.5 MHz Power Amplifier

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This paper presents the design of a power amplifier (PA) for FSK-modulated signals, whose central frequency is 921.5 MHz, made with CMOS 0.35 μm technology. This PA was designed to be part of a system-on-chip (SoC) which will be used in wireless sensor networks.

In the end, three different topologies were proposed: one of which is fully integrated, the second of which has an off-chip output network, and a third one that features external RF chokes in addition to the off-chip output network. These three topologies present trade-offs between performance and integration.

Categories and Subject Descriptors: []: —; []: —

General Terms:

Additional Key Words and Phrases: Power Amplifier, CMOS, RF

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1. INTRODUCTION

This paper presents the design of a power amplifier (PA) which will in turn be part of a system-on-chip (SoC). This particular SoC will be used in wireless sensor networks (WSN) applications, and contains a RF trasnceiver (which contains the PA), a RISC microprocessor, memory, and digital and A/D interfaces [Costa et al. 2005]. The system design followed a top-down procedure. The presented PA is the final component of the RF trasmitter, responsible for providing the necessary power gain to the transmitted signal.

2. SPECIFICATIONS

The proposed power amplifier was supposed to match the following specifications:

—0.35 μm CMOS AMS technology;

—Controllable output power, ranging from 1 to 10 dBm;

—Gain between 15 and 20 dB;

—Power Added Efficiency (PAE) of at least 50%;

—Power consumption smaller than 40 mW;

—The band occupied by the transmitted signal must lie between 915 and 927,5 MHz;

—The transmitted signal shall be a binary FSK-modulated signal, whose simbols are represented by the frequencies 921 and 922 MHz.

The frequency band of the transmitted signal must lie in the ISM band, between 915 and 927,5 MHz. The chosen symbols for the FSK-modulated signal lie near the center of the desired band.

3. PROJECT METHODOLOGY

The adopted methodology to design the PA is composed of three major steps:

—Define specifications

—Choose and simulate a topology

—Design and verify the chip layout

In the first phase, the desired specifications are chosen. The chosen specifications for this project were already presented in section 2.

During the second phase, a PA topology is designed and then simulated. There are quite a few known power amplifer topologies, and the choice among them is based on the defined specifications. Once a topology is chosen, it is then simulated so that it can be known whether such topology performs well or not. If the performance is considered inadequate, then the topology should be reviewed until its simulation results are acceptable. In order to evaluate a given topology performance, the following quantities are calculated: output signal power (P_{out}), defined as the power of the transmitted signal; input signal power (P_{in}), defined as the power of the signal which activates the PA; gain, defined as the ratio between output and input signal power; Power-Added efficiency (PAE); and consumed power (P_{cons}), defined as the power consumed by the entire chip.

Finally, once the topology is approved, we move on to the third phase. During that phase, the physical layout of the chip is designed, verified, and optimized.

4. POWER AMPLIFIER TOPOLOGY

Power amplifier topologies may be divided in two major groups: linear and non-linear topologies. Linear topologies, as the name implies, are topologies whose output signal varies linearly with the input signal. Such topologies are useful when the modulation scheme used demands high linearity. The output signal of non-linear topologies does not vary linearly with the input signal, which may be a serious problem depending on the modulation scheme used. However, non-linear topologies are more efficient than linear ones, and they also preserve the frequency of the input signal. Given that the proposed PA uses FSK modulation, non-linear topologies were

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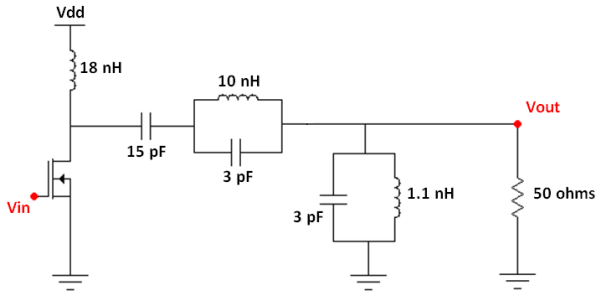

Fig. 1. Chosen topology for the proposed class F Power Amplifier

considered the better choice, since high linearity is not necessary here. For detailed information on PA topologies, the reader is directed to the books by Lee [Lee 1998] and Kazimierczuk [Kazimierczuk 2008].

At first, numerous class E non-linear PA topologies were considered. However, simulation results for those topologies were not as good as the ones for the class F topology shown on figure 1, hence why this topology was chosen. It is a simple 3^{rd} harmonic class F topology, whose simulation results will be shown in section 5. The V_{dd} voltage source shown on figure 1 is a variable DC voltage source, which will be used to control the output power of the PA. The W/L ratio of the transistor in figure 1 is 1000 μm/0.35 μm.

In order to generate the PA's input signal, a VCO was used. This VCO had already been designed [Neves 2010] before work on the PA had begun, and as such, it was treated here as a simple 'black box'. The VCO inputs are two DC voltage signals, named V_{ctrl} and SV_{dd}, which control the frequency of the AC output signal. Since the VCO could not drive the PA's transistor directly, two buffers were used. The schematic for these buffers is shown on figure 2. The RF choke present on figure 2 is a 18 nH inductor (for both buffers), while the W/L ratio of the buffers' transistors is 15 μm/0.35 μm for the first buffer, and 400 μm/0.35 μm for the second buffer.

Figure 3 shows a diagram of all elements present on the proposed system, and table I shows the formulas used to calculate the quantities presented in section 3. Output power was defined as the product of the RMS values of the output voltage and current. Likewise, input power was defined as the product of the RMS values of the input voltage and current. Gain was defined as the difference between output and input power (in dBm). PAE was calculated as the ratio between the diference between output and input power (in watts) and the power supplied by the DC voltage sources feeding the PA and the buffers. The DC power supplied to the VCO was not taken into account, since the VCO is there to generate the signal which will be amplified, and not to amplify it. Finally, the consumed power is defined as the sum of the power supplied by all DC voltage sources, including the power supplied to the VCO, since the consumed power is a measure of all the power consumed by the chip.

5. RESULTS

By the end of the project, we realized that, if we wanted the PA to fully comply with the defined specifications, it would be necessary to abandon the idea of a fully integrated PA and use off-chip components. However, as was stated before, the PA is designed to be used in a SoC, which will be part of a wireless sensor network. As such, the function of each SoC varies. Depending on the desired function for the SoC, a fully integrated PA may still be viable, even

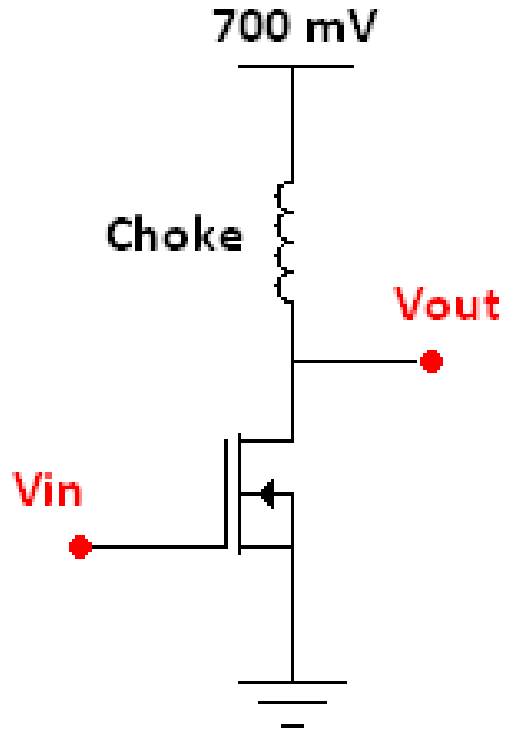

Fig. 2. Buffer schematic

Table I. Simulation parameters

Measurement	Equation
P_{out}	$V_{out}^{RMS} \times I_{out}^{RMS}$
P_{in}	$V_{in}^{RMS} \times I_{in}^{RMS}$
$Gain$	$P_{out}^{dBm} - P_{in}^{dBm}$
PAE	$\frac{P_{out}-P_{in}}{P_{DC}}$, where $P_{DC} = \sum_{i=1}^{M} V_i^{RMS} \times I_i^{RMS}$, M being the number of DC sources feeding the PA and buffers
P_{cons}	$\sum_{i=1}^{N} V_i^{RMS} \times I_i^{RMS}$, N being the number of DC sources feeding the entire chip

if it does not comply with all the defined specifications. In other words, this situation presents a trade-off between performance and system integration.

Three PA topologies are therefore proposed. They are all in accordance with the schematic shown on figure 1: the difference lies in whether they are fully integrated or not. The first topology is a fully integrated PA, and follows the diagram shown on figure 3. The second topology replaces the integrated LC tanks with external ones, in accordance with figure 4. The third topology uses external RF chokes in addition to the external LC tanks. In this topology, both the PA and the buffers use external chokes, as shown on figure 5.

The simulation results for the three topologies are shown on table II. As expected, there is a trade-off between system integration and performance, since the more integrated topologies present worse output power and efficiency, and consume more power than the less integrated ones.

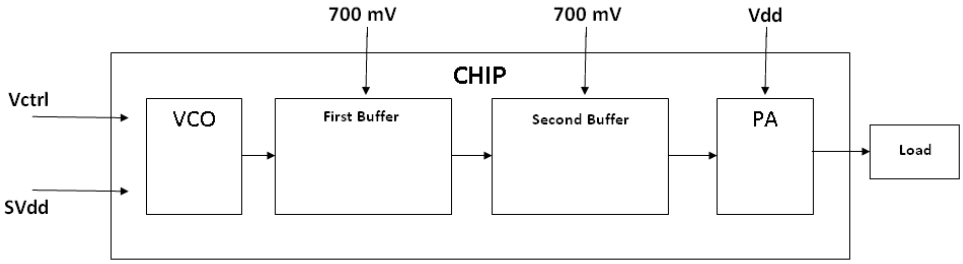

Fig. 3. Fully integrated chip diagram

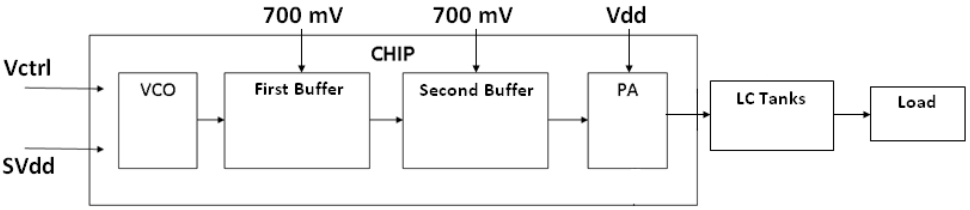

Fig. 4. Chip with external LC tanks

Table II. Simulation results

	First topology	Second Topology	Third Topology
V_{dd}	1,2 V	1,0 V	1,0 V
V_{ctrl}	1,2 V	1,2 V	1,2 V
SV_{dd}	2,4 V	2,2 V	2,2 V
P_{out}	5,963 dBm	7,21 dBm	10,34 dBm
P_{in}	-6,287 dBm	-6,27 dBm	-6,46 dBm
$Gain$	12,25 dB	13,47 dB	16,80 dB
PAE	14,19 %	27,68 %	50,19 %
P_{cons}	32,35 mW	24,34 mW	25,84 mW

The results shown on table II do not take into account post-layout simulations. That is beacause, due to time constraints, only the layout for the third topology was designed. This topology was chosen first because of its higher performance, and the simulation results for the post-layout simultion for that topology are shown on table III, which shows the results for different values of V_{dd}. The designed layout is shown on figure 6.

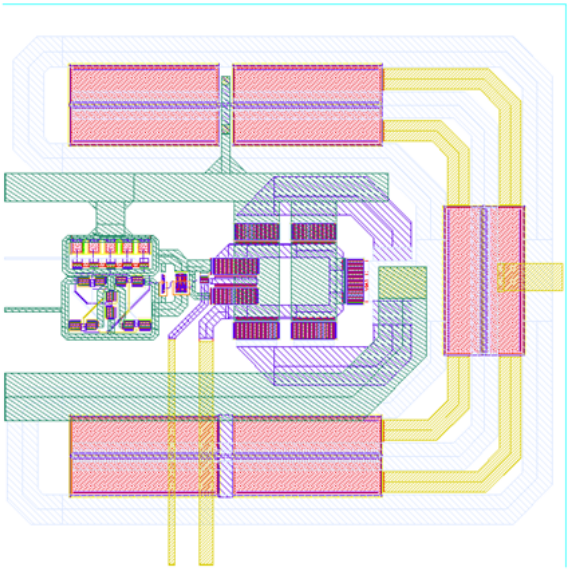

Fig. 6. Designed layout for the third topology

6. CONCLUSION

Three different PA topologies were shown, with varying levels of system integration. These topologies present a trade-off between integration and performance, a relation which must be taken into account by the system designer. Functions which do not demand high performance may benefit from a more integrated approach, while more demanding functions mandate the use of external components.

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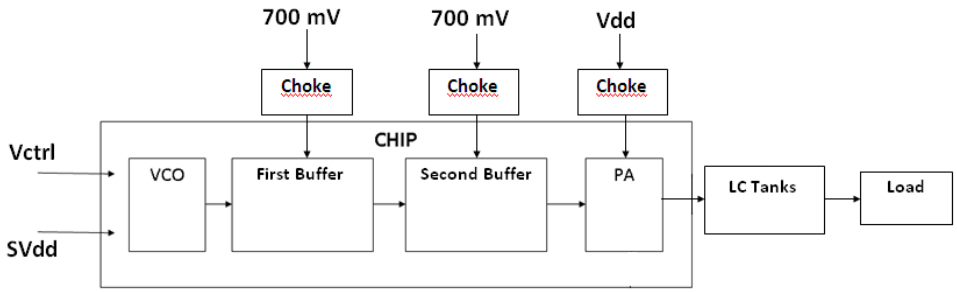

Fig. 5. Chip with external LC tanks and RF chokes

Table III. Third topology post-layout simulation results

$V_{ctrl} = 1,06V$ and $SV_{dd} = 2,5V$						
$V_{dd}(V)$	$P_{out}(dBm)$	$P_{in}(dBm)$	Gain (dB)	PAE (%)	$P_{cons}(mW)$	$f_{out}(MHz)$
0,2	-3,92	-5,04	1,12	2,03	11,66	923,72
0,3	-0,69	-5,04	4,36	9,50	12,79	923,64
0,4	1,62	-5,05	6,66	15,84	14,28	923,55
0,5	3,40	-5,05	8,47	20,78	16,11	923,45
0,6	4,84	-5,05	9,89	24,53	18,25	923,34
0,7	6,05	-5,05	11,11	27,34	20,69	923,22
0,8	7,09	-5,05	12,14	29,47	23,39	923,13
0,9	8,00	-5,06	13,05	31,10	26,33	923,02
1,0	8,80	-5,06	13,85	32,36	29,51	922,95
1,1	9,50	-5,06	14,56	33,34	32,91	922,87
1,2	10,15	-5,06	15,21	34,09	36,51	922,80
1,3	10,73	-5,06	15,79	34,67	40,30	922,73
1,4	11,26	-5,07	16,33	35,11	44,26	922,66
1,5	11,74	-5,07	16,81	35,43	48,38	922,61

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