A new methodology to evaluate the Holding Time in CMOS Logic Gates with Stuck-Open Fault

Alexandra L. Zimpeck, Cristina Meinhardt, Paulo F. Butzen
Universidade Federal do Rio Grande – FURG
Computer Science Center – C3
Rio Grande, Brazil
{alexandra.zimpeck, cristinameinhardt, paulobutzen}@furg.br

ABSTRACT
In nanotechnologies, the behavior of Stuck-Open Fault (SOF) is more affected by the high leakage currents and low signal node capacitance. Therefore, evaluate the holding time is very important because depending on the operation frequency that the circuit is analyzed, some pair of vectors cannot be used to detect a SOF. This work proposes a new methodology to measure the holding time in nanometer technologies. The main objective of the new method is capture the real time when the output switches due to the interaction between leakage currents and stuck open transistor. The correct values of holding time guarantee good test performance and avoid that some faults be electrically masked.

Categories and Subject Descriptors
B.8.1 [**Hardware**]: Performance and Reliability – *reliability, testing and fault-tolerance*

General Terms
Measurement, Performance, Reliability, Experimentation

Keywords
Stuck-Open Fault, Leakage Currents, Holding Time, CMOS Logic Gates

1. INTRODUCTION

During the last decades, integration capacity of integrated circuits (ICs) has increased significantly due to the technology scaling. This evolution happens due to the scaling down of MOS transistors dimensions. At each new technology node, these devices are even smaller and it allows integrating more transistors in a single chip. However, the technology scaling brings up several undesired effects, as variability, aging effects, leakage currents, and also a significant increase in the number of possible faults [1][2].

In this work, the concept of faults is considered as defined in [3], i.e., an unexpected condition that can lead the system to achieve abnormal states. Faults can be originated from design mistakes, physical defects or external interference. This article investigates an electrical characteristic of an open defect type in MOS transistors, called Stuck-Open Fault (SOF). SOF in a single transistor may compromise noise margin, operation speed, and quiescent power supply current [4].

SOFs have been extensively explored in 1980s [5][6]. During the 1990s, the literature on the SOF almost ceased. In recent years, this type of fault becomes a relevant defect mechanism due to the interaction to high leakage currents verified in modern circuits. These high leakage currents in nanoscale technologies influence greatly the well know behavior of SOFs.

Tests for stuck-open faults in CMOS circuits require at least a two-vector sequence. Such test-pairs may be invalidated by delays in the circuit. To test the behavior of the circuits in the presence of faults is indispensable achieving enough period of time to analysis. Test-pairs that are not invalidated by delays in the circuit are known as robust test-pairs. Because of this two factors, SOFs are classified as "sequence dependent, yet timing independent'' (SDTI) failures.

In nanotechnologies, due to the increase of leakage currents and low signal node capacitance, the classical SOF behavior presents an even more complex detection challenge. As the technology reduces, it introduces more variables that further complicate SOF detection [7]. It makes even more important to take into account the delay induced by this kind of fault. Holding Time is a measure related to the delay induced by the SOFs [8]. Determine the holding time is relevant because according to the circuit operation frequency, some outputs can be at the correct electrical level or at an unexpected electrical level.

Champac et al [7] defines the holding time as the time for the output node discharges from V_{DD} to V_{DD} - $|V_{TP}|$, where V_{TP} is the threshold voltage of a PMOS transistor. To transistors NMOS, is the time for output node charges from GND to $|V_{TN}|$, where $|V_{TN}|$ is the threshold voltage of NMOS transistor. Considering that the output capacitance of the logical gate is an inverter, beyond this voltage both load inverter transistors will turn-on and enter in high gain transition region causing a rapid response. By this definition, it is possible to assume that holding time is the time for the output node changes its voltage enough to the next logical level senses this variation and understand this variation at a change in its inputs. However, electrical experiments have showed that those limit values does not causes a switch value in subsequent logic gates and, moreover, this methodology reports very short holding times to SOF detection.

A methodology to increase the robustness of SOF detection controlling the gate leakage at the driven gates is proposed in [9]. In order to improve the holding time observed, this methodology is based in three conditions: I) Minimize the gate leakage current of the turned-on NMOS transistor(s) of the driven gate(s) connected to the high impedance node; II) Minimize the gate leakage current of the turned-off PMOS transistor(s) of the driven gate(s) connected to the high impedance node and III) Minimize (or maximize) the subthreshold leakage current in the NMOS (PMOS) network. This methodology has a strong dependence of the driven gates connected to the high impedance node.

In this paper we propose a new methodology to measure the holding time in static CMOS logic gates with SOFs independently of the driven gate connected to the high impedance node. Therefore, our new method to measure holding time respects the previous definition of the holding time [7], but changes the interval points of measurement. In our methodology, we respect the condition III of the Champac methodology [9] and measure the Holding Time as the time for the output node discharges or charges from V_{DD} to the $V_{TRANSITION}$, where $V_{TRANSITION}$ is the voltage required to the next logical level understand the output signal as an inversion on the logical level.

The article is organized as follows. Section 2 shows the electronic properties of SOFs. The importance of leakage currents in nanometer technologies is discussed in Section 3. Section 4 presents the proposed methodology to measure the Holding Time and compare whit the Champac methodology [7]. Finally, conclusions and futures works are presented in Section 5.

2. STUCK-OPEN FAULT

In normal operation, a transistor makes the connection between two circuit nodes according to the applied signal at the gate terminal. If a SOF happens, it indicates that the connection between two nodes by this transistor will never happen [8], i.e., a charge is prevented from flowing through the transistor when it is activated leading to a high impedance output state (Z).

SOFs are difficult to be tested because the output state depends on the energy load at the output capacitance in previous state. Its detection requires a specific 2-vector pair that examines each transistor in the logic gate for an open defect in device structure.

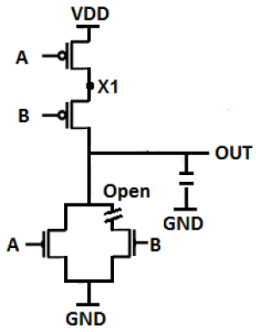
Figure 1 shows a static CMOS NOR2 logic gate with a SOF in transistor B on the pull-down network. In the figure is presented the correct truth table and also the expected truth table with the wrong output caused by the SOFs. In this example, the SOF affects the output with direct dependency of the NMOS transistor with the fault. Always that the output depends on this transistor be on, the output signal will be floating and the output will be in high impedance state (Z), maintaining the signal level store in the node capacitance for a specific time.

Looking at each state of the truth table, we get the following behavior: For the AB=00 vector both the PMOS transistors are turned on, leading to correct output value. The second vector AB = 01, the good transistor in the NMOS network is off and the faulty transistor should be turned on, but cannot supply current to output because of the SOF. Therewith, both pull-down network paths are blocked, making the output signal floats in a high impedance state, maintaining the voltage of the previous state stored in the load capacitance. For the AB = 10 state, the good NMOS transistor is turned on, taking to output the correct logic value. The same results occurs to AB = 11 vector.

One way to simulate the SOF in NMOS device consists in keep the gate terminal with value 0, let the device always open. When the same strategy is applied to PMOS devices, the gate terminal is maintains with value 1, i.e. forcing the transistors PMOS stay open.

3. STUCK-OPEN FAULTS IN NANOMETER TECHNOLOGIES

Stuck-Open fault behavior must be re-examined in nanometer technologies because nano transistors present a significant leakage current and a low signal node capacitance. This behavior is critical during the SOF high-impedance state [10]. Output signal maintains the voltage of the previous state because of the capacitance.



A	B	OUT	OUT*
1	0	1	1
1	1	0	Z
1	0	0	0
1	1	0	0

Figure 1. Stuck-Open fault in a logic gate NOR2 with good (OUT) and bad (OUT*) truth table response

The structure used for analysis of logic gates in presence of faults is shows in Figure 2. In this experiment, a logic gate is connected in an inverter chain and the signal output is observed in OUT and INV1. This structure aims highlight the influence of SOF in the next logical stage. The transistor sizing is defined by logical effort [11]. In the experiments, we use four nanometer technologies from Berkeley Predictive Transistor Model [12]: 16nm, 22nm, 32nm and 45nm. All simulations were performed in electrical simulator NGSpice [13].

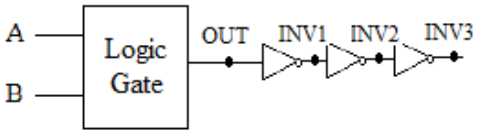


Figure 2. Logic Gate with Inverters

First, we used the NOR2 gate to verify circuit behavior with SOFs. To analyze the high impedance behavior of SOF in a NOR2 gate in four technologies it is needed evaluate the behavior when the fault occurs in pull-down network, i.e. in the network where transistors are in parallel arrangement. Faults in series transistor arrangements have always the same behavior, an incorrect output. To test the high impedance behavior in a NOR2 gate, when the fault is inserted in the transistor A of the pull-down network, the robust test-pair is $00 \rightarrow 10$. But when the fault is in transistor B, the robust test-pairs is $00 \rightarrow 01$.

Figure 3 illustrate the behavior of the NOR2 gate in presence of fault to four technologies. It can be seen that the output is held in the last state for a short time. This time reduces according with the technology scaling down. This happens because in smaller technologies, larger are the leakage currents.

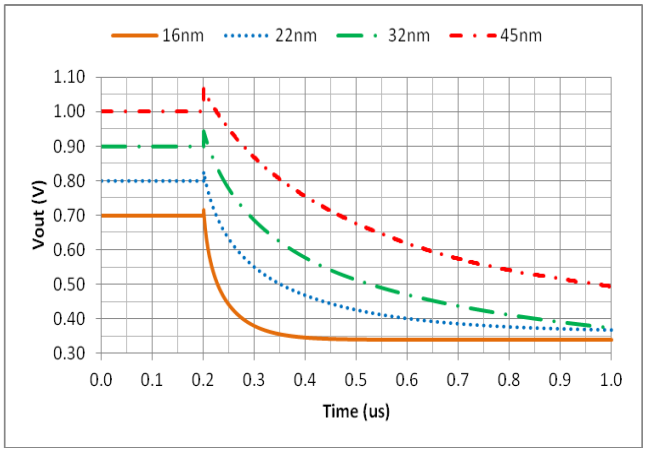


Figure 3. Obtained result for a NOR2 gate with SOF in transistor B at the 16nm, 22nm, 32nm and 45nm technologies

In second, we utilize the NAND2 gate, which have complementary behavior. The influence of SOFs in the four technologies is only verified at pull-up network. When the fault is inserted in transistor A, the pair of vector affected is 11 → 01. When the fault is in transistor B, the pair of vectors is 11 → 10.

4. HOLDING TIME BEHAVIOR

Figure 4 exemplifies the influence of SOF in next logic stages, for a 32nm technology. The output signal falls slowly because the output is in high impedance. The next logic stage only achieves the expected value after a delay due to the interaction between high leakage currents and SOF. The holding time is a way to measure this delay induced by the SOF to exchange the input state of the next stage.

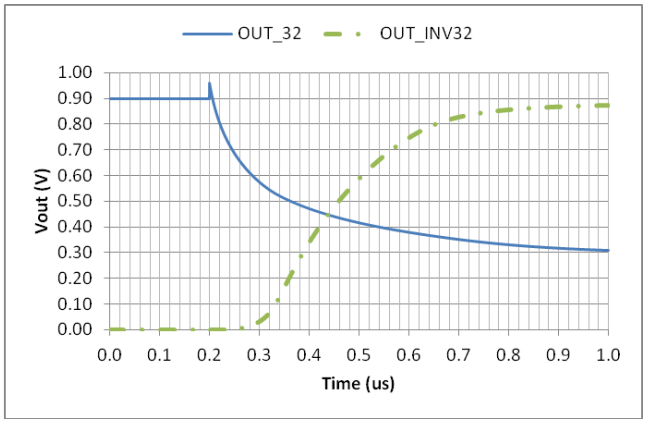


Figure 4. Obtained result with SOF inserted in transistor A at the NOR2 gate in technology 32nm

It is necessary to determine the holding time because moderns circuits have very high leakage currents. The holding time was simulated for different scaled technologies and the results are shown in Figure 5 and Figure 6. Holding time reduces as technology is scaled due to increased leakage and smaller node capacitances. Therefore, for nanotechnologies, depending on the frequency that the circuit is operating, it may contain a wrong result,. To avoid this fail detection, the operation frequency has to be defined according to the holding time.

Considering the NAND2 and NOR2 gate, it was made an experiment measuring the holding time as defined in [7] and according to proposed methodology. Both logic gates have two pairs of test vectors in which the behavior of the fault can be observed. The pair of vectors with high holding time is defined as the robust test pair to measure holding time in nanotechnologies.

The reference [7] measure the Holding Time of a NOR2 gate as the time for the output to discharge from V_{DD} to V_{DD} - $|V_{TP}|$, where $|V_{TP}|$ is the PMOS transistor threshold voltage. For a NAND2 gate, when the fault affects the pull-down network, the holding time is the charging time for output would be from GND to $|V_{TN}|$, where $|V_{TN}|$ is the threshold voltage of NMOS transistor. For effect of simplicity, in all analyses we are considering $|V_{TP}| = |V_{TN}| = 0.3$ V as a technology free abstraction.

Giving this definition and observing the SOF behavior on nanotechnologies described in Figure 4, we can see that the holding time measured as [7] is a very short time compared to the time need to the next logic stage change his state.

The new methodology propose in this work for measure the holding time recommends to measure the holding time as the time need to the next logic stage change its state after a transition on the fault circuit. By this methodology, the holding time is now the time for the output discharges from V_{DD} to $V_{TRANSITION}$, where $V_{TRANSITION}$ is the voltage required to the next logic stage understands the output signal as an inversion on the logic level. We are assuming $V_{TRANSITION}$ as $V_{DD}/2$. With this new approach the holding time increases, i.e., increases the time in that output is considered to remain in previous state. It increases the time that the tester should have to detect SOF in static CMOS circuits.

The robust test pair to measure holding time for the NOR2 gate with a SOF is the pair 00 → 10 and the results for the two ways of measure the holding time is showed in Figure 5.

For NAND2 gate, the values obtained measuring the holding time with the two approaches is showed in Figure 6. The robust test pair of the vectors with high Holding Time is the pair 11 → 10.

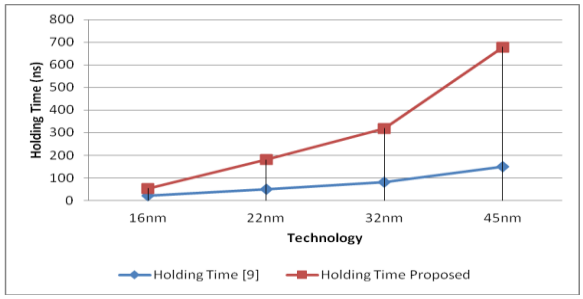


Figure 5. Holding Time in the NOR2 gate

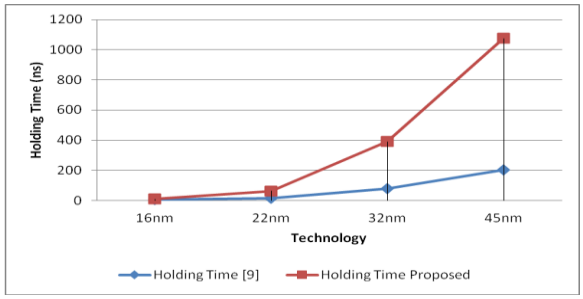


Figure 6. Holding Time in the NAND2 gate

4.1 Analysis the Holding Time for different Fan-Out in New Method

The holding time also depends on the load capacitance on the output and on the paths from the output to V_{DD} or GND. Table 1 shows the holding time dependence of the number of load inverters at the output.. It was simulated against fan-out for a number of load inverters at the output. This table shows the effect of fan-out on high-impedance state response for the four technologies evaluated. The holding time proposed and as defined in [7] was measured for the NOR2 and NAND2 gates with different fan-out.

The conventional holding time as defined in [7] increases as the number of inverters connected in OUT increases [9]. Obtained results with NOR2 and NAND2 gates show the same behavior for the holding time measured according our methodology. These values were obtained considering the robust test-pairs of each gate, i.e., the fault is inserted in the transistor B in pull-down network in NOR2 gate and in the transistor B in pull-up network in NAND2 gate. A first analysis about the fan-out shows the holding time increases as the number of inverters connected to the output increases, i.e, holding time increases for large fan-outs.

With the new methodology proposed in this work, the holding time increases significantly for all technologies. The increase is described by the ΔHT value in Table 1. As to test the behavior of the circuits in the presence of SOFs is indispensable achieving enough period of time to analysis, our methodology results point to increase the robustness of SOF detection

5. CONCLUSION AND FUTURE WORKS

Stuck-open faults became more complex with the technology scaling. The SOF behaviors are modified with the increase of leakage currents and the reduction of signal node capacitance. Nowadays, static CMOS gates with SOF have a behavior that combines the classical and non-classical responses for fault circuits, and this behavior is function of clock period, fan-out, leakage current, noise, V_{DD}, and temperature.

In this work we focus on proposes a new method to measure the holding time to capture the real time to cause a switch in next logic stage. For nanotechnologies, conventional holding time measurement method [9] reports a strategy that does not reflect that switch. It can be concluded that with this new method of measuring Holding Time is possible to guarantee the fault detection when this holding time constraint is respected. And, the results suggest the adoption of slower clock periods to increase the chances of error detection.

As future work, we will analyze the behavior of Holding Time in other circuits and extend our study to consider the impact of V_{DD}, noise and temperature variation in the SOF behavior and holding time.

6. ACKNOWLEDGMENTS

This project was financially supported by the scientific initiation program (PIBIC) of Universidade Federal do Rio Grande – FURG

7. REFERENCES

[1] L. Anghel and M. Nicolaidis, *Defects Tolerant Logic Gates for Unreliable Future Nanotechnologies*, Lecture Notes in Computer Science, v. 4507, Berlin, 2007, pp. 422-429.

[2] A. L. Zimpeck, C. Meinhardt and P. F. Butzen, *A tool to Evaluate Stuck-Open Fault in CMOS Logic Gate*, Simpósio Sul de Microeletrônica (SIM), 2013.

[3] D. T. Franco, *Fiabilité Du Signal des Circuits Logiques Combinatoires sous Fautes Simultanées Multiples*, Doctoral Thesis, I'École Nationale Supérieure des Télécommunications, França, 2008.

[4] W. W. Needham, C. Prunty and E. H. Yeoh, *High volume microprocessor test escapes, an analysis of defect our test are missing*, in Proc. 1998 Int. Test Conf., 1998, pp 25-34.

[5] R. Wadsack, *Fault modeling and logic simulation of CMOS and MOS integrated circuits*, Bell Syst. Tech., pp. 1449-1488, May-Jun, 1978.

[6] J. Soden, K. Treece, M. Taylor and C. Hawkins, *CMOS IC stuck-open fault electrical effects and design considerations*, In Int. Test Conf., Aug. 1989, pp. 423-430.

[7] R. Gomez, V. Champac, C. Hawkins and J. Segura, *A Modern Look at the CMOS Stuck-Open Fault*, IEEE LATW, 2009.

[8] G. V. Pereira, *Teste da rede de Interconexões de Field Programmable Analog Arrays*, Master Thesis, PPGC, UFRGS, Porto Alegre, 2005.

[9] R. Gomez, V. Champac, C. Hawkins, J. Segura, S. Barceló and J. V. Hernández, Testing of *Stuck-Open Faults in Nanometer Technologies*, IEEE Design & Test of Computers, 2012.

[10] A. Keshavarzi, K. Roy and C. Hawkins, *Intrisic leakage in low power deep submicron CMOS IC's*, International Test Conference, pp. 146-155, 1997.

[11] Ivan E. Sutherland and Robert F. Sproull. "Logical effort: designing for speed on the back of an envelope." *IEEE Advanced Research in VLSI* (1991): 1-16.

[12] Y. Cao, T. Sato, D. Sylvester, M.Orshansky, C. Hu., "New paradigm ofpredictive MOSFET and interconnect modeling for early circuit design," *Proc.IEEE Custom Integrated Circuits Conference*, pp. 201-204, 2000.

[13]NGspice. [Online]. Available: http://ngspice.sourceforge.net/.

Table 1. Holding Time for different fan-out for NOR2 and NAND2

Logic Gate	Fan-out	16nm			22nm			32nm			45nm		
		[7] (ns)	New (ns)	ΔHT (%)	[7] (ns)	New (ns)	ΔHT (%)	[7] (ns)	New (ns)	ΔHT (%)	[7] (ns)	New (ns)	ΔHT (%)
NOR2	**3**	24,68	42,77	73,29	55,56	174,80	214,61	82,27	325,46	295,59	153,50	746,21	386,13
	4	31,09	54,06	73,88	69,35	221,86	219,91	102,05	412,74	304,44	185,25	938,80	406,77
	5	37,49	65,33	74,25	79,24	303,07	282,47	121,64	499,47	310,61	214,85	1127,07	424,58
NAND2	**3**	6,71	15,35	128,76	25,89	91,41	253,07	123,87	704,70	468,90	280,70	1821,37	548,86
	4	7,95	18,40	131,44	30,42	110,60	263,57	145,36	862,04	493,03	313,54	2145,16	584,17
	5	9,19	21,46	133,51	34,95	129,79	271,35	166,70	1019,18	511,38	342,89	2441,93	612,16