On a multi-finger multi-tube common source sub 50 nm CNTFET amplifier

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***Abstract*—Carbon nanotube (CNT) field-effect transistors (FETs) are an attractive technology for high-speed analog device applications due to their high intrinsic transconductance and very low capacitance per tube. First high-frequency devices with moderate layout dimensions based on random multi-tube networks will soon be available commercially. We report here on the design and simulation of a common source amplifier with 100 CNTs in parallel employing 20 gate fingers. The presented study is one of the first demonstrations of the newly developed TCAM compact model for multi-finger multi-tube ballistic CNTFETs which has been successfully implemented in the commercial Spectre SPICE-class circuit simulator. Catalytic growth of CNTs leads typically to an undesired ratio of semiconducting to metallic tubes of 2 to 1. We analyze the degradation of the voltage gain of the common source amplifier due to the metallic tube fraction.**

Keywords: CNTFET, multi-finger, multi-tube.

I. Introduction

Silicon is the most commonly used material for connecting source and drain terminals in a FET transistor. However, recent experimental and theoretical results suggest that carbon nanotube (CNT) field-effect transistors (FETs) are a promising option to replace silicon based transistors at least for analog applications, providing higher linearity, lower noise and high thermal stability [1]. CNTFETs may offer also advantages for digital applications like lower power, faster and smaller circuits [2], [3]. Carbon nanotubes are formed by graphene rolled sheets [4]. Their structure is hexagonal and, depending on the chirality of the wrapped sheet, determines whether the nanotube is metallic or semiconducting [4].

As nanotubes have a high current carrying capability (approximately $104\,\mathrm{mA/\mu m^2}$ [1], placing hundreds of CNTs in parallel between source and drain leads easily to transistors with sufficient output power for analog applications. Therefore, CNTFETs for analog circuit design are multi-tube FETs. To reduce the gate resistance, usually multiple gate fingers are employed. Main layout parameters for a multi-finger multi-tube CNTFET technology are the gate width and the number of gate fingers. In the present paper, we fix the gate width to 10 μm leading to a transistor channel formed by 100 parallel CNTs (for a given nanotube density of $10\,/\mu\mathrm{m}$). A CNT density as high as possible would be desirable to reduce the impact of layout parasitics. The current transport through CNTFETs is limited by Schottky barriers (SB) at the interface between the metal contacts and the channel and by scattering within the channel. Both phenomena affect the bias dependence of the current and of the charges and, thus, of the small signal quantities of the transistor. For SB CNTFETs with a channel length of below $50\,\mathrm{nm}$, the Schottky barriers dominate the transport and the impact of scattering can be neglected in leading order. Hence, transport along the channel is assumed to be ballistic, which limits the investigations presented here to short channel lengths (up to $50\,\mathrm{nm}$).

Catalytic growth of CNTs typically leads to a fraction of metallic tubes of 30%, since their diameter cannot be controlled. Nevertheless, CNTFETs with metallic tubes in the channel still exhibit acceptable intrinsic properties. However, already in simple circuits such a high fraction of metallic tubes may not be tolerable. As we will demonstrate in the present paper, already a metallic fraction of 8% is sufficient to render the design of a common-source amplifier impossible. Note however, that the raised issue applies only to short-channel ballistic transistors. For longer channels, the resistance of metallic tubes is much higher and therefore their impact smaller.

To evaluate the potential of an emerging and prototype (such as CNTFET) technology, circuit design studies are very important. However, compact models for such technologies, which are essential for circuit design and simulation, are rarely available and are most often not fully developed. Thus, the possibilities for the circuit designer regarding e.g. scaling, temperature and statistical studies are restricted and the bias and frequency regions have to be chosen with care to not contradict the assumptions under which the model was developed and for which the model gives reliable results. A few physics-based CNTFET compact models have been already published (e.g. [5]–[9]) and are critically reviewed in [10]. It turned out that they are not suited for analog circuit design for several reasons (see [10]). In the absence of a suitable physics-based compact model, the best option for enabling analog RF circuit design and CNTFET technology evaluation appears to be the use of empirical formulations such as those in [11]. The model in [11] is dedicated to the design of analog high-frequency CNTFET circuits for already available CNTFET process technologies

with channel length of around 800 nm. However, due to the empirical base, the model does not allow an insight into the relevant parameters, which impacts the transistor and circuit behavior, and is therefore only of limited use for supporting the CNTFET technology development and optimization process.

For the circuit design study in this paper a different model, TCAM, is employed. TCAM is a recently developed (by one of the authors: M.C.) compact model for SPICE like simulators and all results given here are Calibre simulations. The model employs simplified equations to calculate the non-equilibrium charge densities and currents as result of injected carriers at the contacts including near-contact potential barriers. TCAM is based on the transmission-based compact model for semiconducting single-tube CNTFETs proposed in [12] but has been extended towards a multi-tube compact model including all relevant transistor parasitics and metallic tubes. For the latter, scattering effects are included according to the equations used in [13], [14]. The model was verified by comparison with a full in-house Schrödinger-Poisson solver, simulating a CNTFET with a 1d transport channel in a 3d electrostatic environment. TCAM is a model for a sub 50nm CNTFET technology and the semiconducting tube parameters of the model were fitted to the experimental results published in [15]. For circuit designer the most relevant model parameters are the gate width and the number of gate fingers. The model also allows changing the tube density and the fraction of the metallic tubes. This gives the circuit designer access to some critical technology parameters and opens e.g. the opportunity to analyze the scaling potential of a given technology. Further details concerning TCAM will be published elsewhere.

The usage of CNTFETs in analog circuits has been increasingly investigated in the recent literature [16], [17]. As one of the first design examples based on the newly developed TCAM compact model for multi-finger multi-tube ballistic CNTFETs, we present here a simulation study of a common-source amplifier, which is suitable for the use in amplifiers of transmitters and receivers of wireless transmission technologies.

II. TRANSIT FREQUENCY

An important figure of merit for high-speed transistors is the transit frequency f_T, which can be derived from a simulation of the transistor's Y-parameters. In accordance with the experimental procedure, we extract the Y-parameters at a frequency of $f = 1\,\mathrm{GHz}$. The gate capacitance $C_\mathrm{g} = C_\mathrm{gs} + C_\mathrm{gd}$ consists of a drain $C_\mathrm{gd} = -\mathrm{Im}(Y_{12})/2\pi f$ and source $C_\mathrm{gs} = \mathrm{Im}(Y_{11} + Y_{12})/2\pi f$ contribution. Then, from the transconductance

$$g_m = \sqrt{\mathrm{Re}^2(Y_{21} - Y_{12}) + \mathrm{Im}^2(Y_{21} - Y_{12})}$$

the transit frequency is obtained:

$$f_\mathrm{T} = \frac{g_m}{2\pi\, C_\mathrm{g}} \tag{1}$$

We investigate the dependence of f_T on the fraction of metallic tubes in Fig.1. As can be seen, the modeled multi-finger multi-tube CNTFETs can reach maximum cut-off frequencies in the low THz regime. Although the transit frequency decreases significantly with the fraction of metallic tubes, f_T keeps high values, in the order of 400 GHz for a metallic tube fraction of 10%. Lower values of f_T indicate a lower transconductance g_m and/or a higher CNTFET internal gate capacitance. The metallic tubes represent a parasitic conducting channel in parallel to the semiconducting one and indeed introduce additional capacitances. Also the transconductance decreases slightly with the metallic tube fraction. The number of gate fingers has no impact on the transit frequency (not shown here).

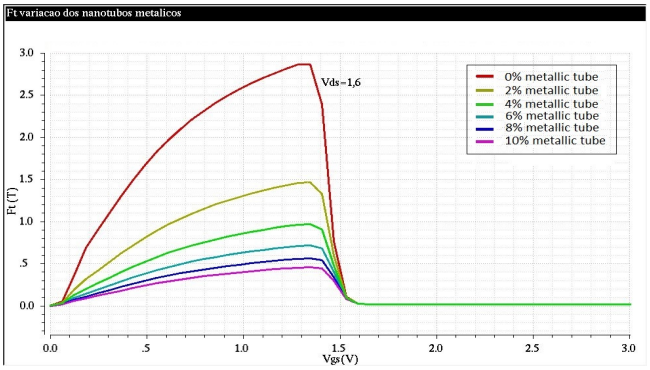

Fig. 1: Transition frequency (f_T) versus V_gs, the employed drain bias is $V_\mathrm{ds} = 1.63\,\mathrm{V}$.

III. COMMON-SOURCE AMPLIFIER

The parameters of the TCAM compact model and their values employed here are: Gate width $W_\mathrm{g} = 10\,\mu\mathrm{m}$, number of gate fingers $n_f = 20$, nanotube density $\rho_\mathrm{CNT} = 10\,/\mu\mathrm{m}$ and a metallic fraction of $m_f = 0\%, ..., 10\%$. In the present work, we focus on the impact of the metallic tube fraction, a technology parameter, on the performance of a common-source amplifier. The reasons are twofold. First, the presence of metallic tubes is currently still unavoidable. Obviously, it would be desirable that all CNTs have semiconducting properties. However, due to limitations in the fabrication process, approximately 30% of nanotubes have metallic properties. Many research works have been devoted to reduce the metallic tube fraction, but a suitable method for a transistor process technology has not been found so far. Second, the impact of metallic tubes has to be expected to increase for a scaled technology providing shorter channel lengths. The longer the distance between source and drain, the larger is the resistance of the metallic tubes. In the present paper, as the modeled ballistic transistors have reduced dimensions, a small percentage of the metallic nanotubes almost induces an ideal short-circuit, and a fraction of 10% of metallic CNTs substantially degrades the performance of the amplifier.

A. Analysis of DC characteristics

To identify a suitable DC bias point, the voltage transfer curves (V_ds versus V_gs) of the CNTFET has been simulated for various values of the drain resistance and a supply voltage of $V_\mathrm{pol} = 3\,\mathrm{V}$. The transfer curve for a drain resistance of $10\,\mathrm{k}\Omega$

is given in Fig. 2. For each transfer curve the DC operating point was chosen to maximize the slope for a fraction of 0% of metallic nanotubes. In the given transfer curve of Fig. 2 the DC bias point amounts to $V_{\mathrm{gs}} = 0.5\,\mathrm{V}$ and $V_{\mathrm{ds}} = 1.63\,\mathrm{V}$ leading to a small-signal voltage gain of $A_v = 14.5\,\mathrm{dB}$. As it turned out, the same gate bias maximizes approximately also the slope for CNTFETs with a finite fraction of metallic CNTs. However, higher metallic fractions result in reduced values of V_{ds} and A_v at the given gate voltage. We analyzed

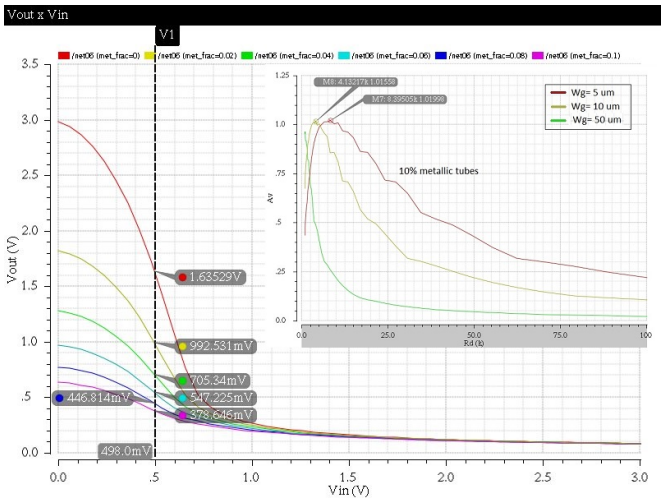

Fig. 2: Voltage transfer curve V_{out} ($= V_{\mathrm{ds}}$) vs. V_{in} ($= V_{\mathrm{gs}}$) for a drain resistance of $R_0 = 10\,\mathrm{k\Omega}$ and CNTFETs with various metallic tube fractions. Inset: Maximum voltage gain A_v as function of the drain resistance R_0 for a CNTFET with a fraction of metallic tubes of $m_f = 0.1$.

the variation of the gain A_v with the resistance R_0 for three different W_{g} values: 5 µm, 10 µm and 50 µm for the ideal case with no metallic nanotubes and for an increasing fraction of metallic nanotubes until 10%. The maximum voltage gain without metallic tubes varies with R_0 and W_{g}. For a specific R_0 value, the higher the gate width, the higher the voltage gain will be and vice versa, for a specific value of W_{g} (i.e. a specific number of CNTs connecting drain and source), the higher the R_0, the higher the voltage gain. As a matter of fact, this is a well-known relation between the voltage gain and R_0 in MOS transistors ($A_v = -g_m R_0$). Nevertheless, it is interesting to notice that the behavior of the same CNTFET transistor for 10% of metallic tubes is quite different. The inset of Fig. 2 demonstrates the dependence of the maximum voltage gain on the gate resistance for a CNTFET with a metallic tube fraction of $m_f = 0.1$. It can be seen that after the maximum voltage gain, the higher the Wg, the lower the voltage gain is. This low voltage gain is a consequence of the shorts between source and drain caused by the metallic tubes. With higher gate widths (at a given fixed tube density) also the absolute numbers of metallic tubes connecting drain and source increase. For the following investigation we choose a value of $R_0 = 10\,\mathrm{k\Omega}$, since the common-source amplifier shows a voltage amplification (albeit very small) even for a finite amount of metallic tubes. For a CNTFET technology, which could eliminate all metallic tubes a higher value of R_0 would be preferable and voltage gains of 26 dB are easily achievable.

For the common-source amplifier proposed in Fig. 3, a supply voltage of $V_{\mathrm{pol}} = 3\,\mathrm{V}$ and a drain resistance of $R_0 = 10\,\mathrm{k\Omega}$ has been employed. The values of the resistances of the voltage divider at gate amount to $R_1 = 100\,\mathrm{k\Omega}$ and $R_2 = 21.36\,\mathrm{k\Omega}$. For an ideal CNTFET with no metallic tubes the corresponding DC bias point equals to $V_{\mathrm{gs}} = 0.5\,\mathrm{V}$, $V_{\mathrm{ds}} = 1.63\,\mathrm{V}$ and $I_{\mathrm{d}} = 0.14\,\mathrm{mA}$.

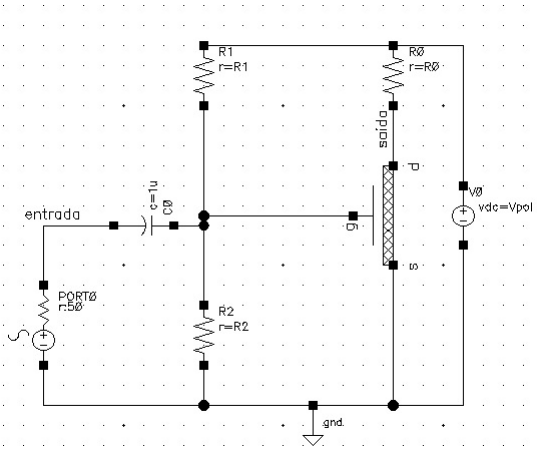

Fig. 3: Common-source CNFET amplifier circuit.

In summary, with a pure semiconducting channel a considerable (quasi static) voltage gain of 14.5 dB could be achieved. However, already small fractions of metallic tubes degrade the performance of the common-source amplifier. We will investigate now, up to which frequencies the gain remains stable.

B. Frequency analysis

Using the DC operating point determined in section A, a small AC signal was applied to the input. With the given value of R_0, the high frequency response of the common-source amplifier for different values of the metallic tube fraction was simulated (Fig. 4). A 1 µF capacitor was connected to the input terminal. The amplifier circuit keeps the voltage gain constant for each metallic tube fraction until approximately 3 GHz. For higher frequencies, there is a convergence of all curves to 0 dB, which can be explained by the fact that the internal transistor capacitance between drain and source are short-circuited, and all curves converge to the same zero gain, independently of the metallic tube fraction. In respect to Fig. 4 it should be noted, that only frequencies below the transit frequency of the corresponding CNTFETs would be employed. Moreover, no impedance matching at the output has been considered.

The number of gate fingers (all parallel) defines an effective gate length. Therefore, the higher the number of fingers, the higher the area and the lower the gate resistance will be. In other words, the number of fingers is inversely related to the gate series resistance. For low frequencies, the number

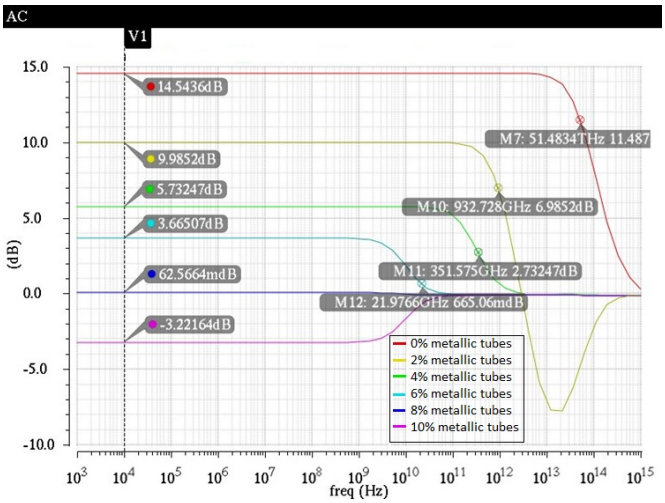

Fig. 4: Maximum voltage gain A_v as function of AC frequency. The gain of an ideal CNTFET remains stable even beyond the transit frequency of the transistor. The gain of CNTFETs with metallic tubes degrade before reaching the transit frequency.

of fingers has no significant influence because no significant current enters the gate. However at high frequencies the gate series resistance will degrade the voltage gain. The effect can be reduced by using a larger number of gate fingers (not shown here).

IV. Conclusion

The scaled (50 nm channel length) CNTFET technology considered in the present paper holds the promise of high-speed analog applications well into the upper GHz regime. While presenting interesting advantages, circuit design tends still to be quite similar to the one based on current MOS technology. Future design activities may explore different architectures to fully evaluate the potential of CNTFET technologies. Moreover, circuit design and simulation for such an emerging technology gives also valuable input for the challenges, which the technology has to overcome, before entering the market. From the design point of view, there are some solutions that can be used to make the CNTFET circuit operate at high frequencies, such as increasing the number of fingers. In this paper, we showed that for a simple amplifier circuit, CNTFETs present good gains reaching values above 20 V/V (26 dB) and a steady frequency response well into the upper GHz regime. A 50 nm MOS transistor would not operate at such high frequencies. However, the performance of the common-source CNTFET amplifier will be considerably limited by a finite fraction of metallic tubes. For channel lengths of 50 nm and below, phonon scattering of the charge carriers within the channel can be neglected. Therefore, the resistance of undesired metallic nanotubes connecting drain and source is very small, approaching a ballistic conductor, so that there are little short circuits between source and drain, degrading the circuit response. As a consequence, a successful design of a common-source amplifier is only possible, if the technology eliminates the metallic tube fraction. It should be noted that the drawn conclusion is only valid for the scaled technology considered here. For larger transistors, the metallic tube resistance becomes higher, reducing its effect on the CNFET performance.

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