ANALYSIS OF SHORT CHANNEL EFFECTS IN TRIPLE-GATE JUNCTIONLESS NANOWIRE TRANSISTORS WITH DIFFERENT DOPING CONCENTRATIONS

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ABSTRACT

This work studies the influence of the total channel length in junctionless nanowire transistors (JNT) through three dimensional simulations. It will be considered a wide range for this dimension and two different doping concentrations, in order to analyze the occurrence of short channel effects (SCE). This evaluation study will use the threshold voltage, subthreshold slope and Drain Induced Barrier Lowering as figures of merit to check on short channel effects.

1. INTRODUCTION

Silicon-On-Insulator (SOI) technology has brought many improvements to the bulk transistors, which were replaced by SOI devices due to the significant reduction of the junction capacitances and reduced short-channel effects, for example [1]. However, attending the expectations of Moore's law and nanotechnology progress consists in incessant improvements and development, which are extremely related to scaling down devices dimensions as much as possible, without losing performance by undesirable effects, such as short channel effects [2].

Since of then, many different tridimensional structures were created in association to SOI technology. For example, multiple gate transistors were designed in order to increase the electrostatic charge control, in the channel region, by the gate contact [3]. This better control over the channel allowed reduced short channel effects and, as consequence, a higher scaling down of these transistors, once a shorter channel length is needed to degrade the characteristics in comparison to planar devices.

Despite of this improvement, scaling down transistors to dimensions of a few nanometers became very complicated, because of difficulties in fabrication process to create very abrupt junctions between drain to channel and source to channel. That motivated the development of junctionless nanowire structure, which has a uniform and high constant doping concentration profile along the stripe of silicon, solving the problems of creating sharp junctions [4].

JNT operation is quite different of the others nMOSFETs, which generally operate in inversion mode (IM). Due to its thin silicon thickness and high doping concentration, junctionless transistor remains totally depleted without gate to source voltage applied (V_{GS}=0V), so it is turned off and there is no current flowing, since a depleted region has no free carriers. When applied an increasing positive gate voltage, the depletion region starts to reduce and a channel is constituted, allowing current to flow, so the device is turned on. Initially, current flows through the body and there is a partially depleted conduction mode. Then, after applying a gate voltage higher than the flatband voltage (V_{FB}), carriers accumulate at surface and there is current flowing through both body and surface [5].

Figure 1 shows the perspective and the cross-section illustration for both standard (IM) and JNT SOI nMOSFET.

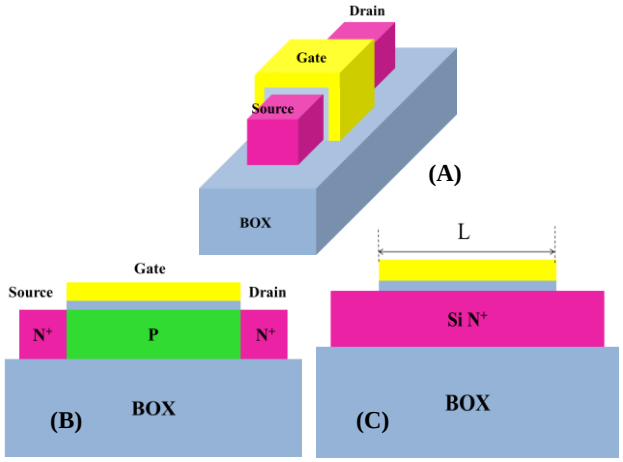

Figure 1 – Standard (IM) and JNT perspective (A) and Standard (IM) (B) and JNT (C) SOI cross-section.

In this study the occurrence of short channel effects in junctionless transistors with two different doping concentrations will be analyzed according to their channel length reduction. The comparison will be performed considering the threshold voltage roll-off, subthreshold slope degradation and Drain Induced Barrier Lowering as figures of merit of SCE.

2. PHYSICAL CHARACTERISTICS AND SIMULATOR

The triple-gate junctionless devices have been simulated presenting uniform N-type doping concentrations of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$ in channel region and P-type polysilicon as gate material. Besides that, all transistors have the geometrical dimensions indicated in Table I, as represented in Figure 2.

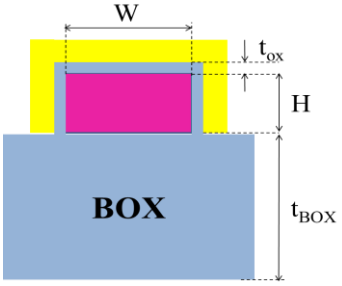

Figure 2 –Front view of Junctionless SOI nMOSFET.

Table I – Junctionless transistors physical dimensions used in simulations.

Parameter	Dimension [nm]
Gate oxide thickness (t_{ox})	2
Buried oxide thickness (t_{BOX})	100
Fin width (W)	20
Fin height (H)	10
Source and drain length (L_{SD})	20
Total channel length (L)	from 30 to 1000

The three-dimensional numerical simulations have been performed with Sentaurus Device Simulator, from Synopsys. This simulator uses the finite element method to solve continuity and Poisson equations [6].

In these simulations, it has been considered different models, which describe the carriers' mobility dependencies on the doping concentration, temperature, normal electric field, velocity saturation of the carriers in high electric fields, dependence of the bandgap narrowing and recombination on the doping concentration. For all the simulations the temperature was set at 300K.

3. RESULTS

3.1. Short channel effects investigation

Figure 3 shows the drain current (I_{DS}) as function of the gate voltage (V_{GS}), when applied a low electric field at drain, V_{DS}=50mV, for junctionless transistors simulated with N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$ and several different channel lengths (L=30, 40, 50, 60, 80, 100, 125, 250, 375, 500, 625, 750, 875 and 1000nm). For smaller values of L, was used a step size of 10nm, then it increased to 20nm, 25nm and, finally, 125nm when L is large enough to avoid short channel effects. It was used a low drain voltage to extract the threshold voltage (V_{TH}) and the subthreshold slope (S). Moreover, to compare the influence of the different doping concentrations, the same scale for I_{DS} was used in both graphs.

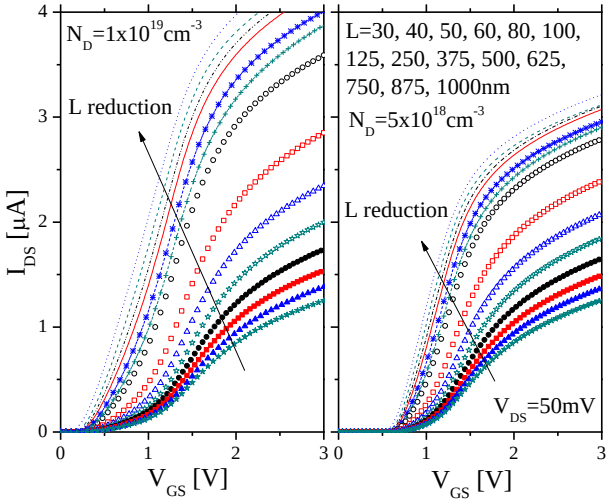

Figure 3 – I_{DS} versus V_{GS} curves for JNTs with L from 30 to 1000nm, N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$ and V_{DS}=50mV.

From Figure 3, one can note the increase of drain current with channel length reduction, which is explained by the inverse relation between these parameters, which is very well known in literature, because of the channel resistance associated to the current flowing. Furthermore, the drain current increases with higher doping concentration, due to the higher carrier mobility in highly doped JNTs [2].

It can be seen a strong degradation of I_{DS} characteristic for gate voltage higher than 2V, approximately, because of high series resistance values found in these devices [7].

From these results, the threshold voltage (V_{TH}) was extracted for each one of the JNT, through the g_m/I_D method, where V_{TH} corresponds to the gate voltage for the half of g_m/I_D maximum value [8]. In order to analyze the influence of N_D and L over V_{TH}, Figure 4 shows the results for simulated JNT as a function of the channel length, with V_{DS}=50mV and V_{TH} calculated according to the model proposed by Trevisoli, et al. [8].

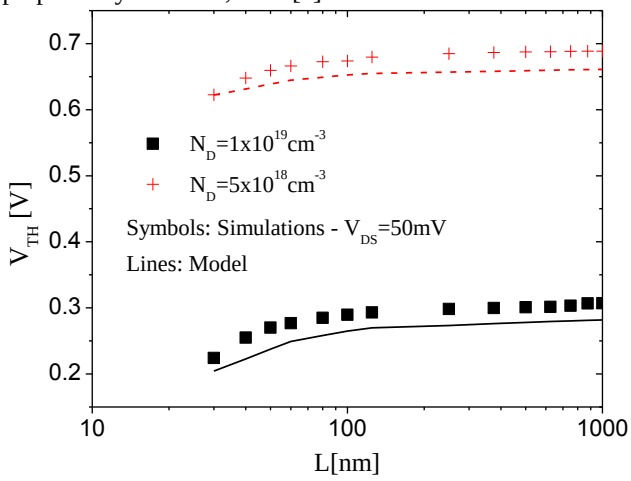

Figure 4 – V_{TH} versus L results for simulations and model of JNTs with N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$.

Figure 4 shows a clear degradation of the V_{TH} values for devices with a channel length shorter than 80nm. Considering $N_D=1\times10^{19}cm^{-3}$ there is a degradation of 82.8mV for simulated V_{TH} between 30nm and 1000nm of channel length, which is 27% of the maximum value (V_{TH}=0.30V). For JNTs with $N_D=5\times10^{18}cm^{-3}$, it is observed higher threshold voltages and a degradation of 66.1mV, which is lower such in magnitude as in comparison to the maximum value (V_{TH}=0.69V).

According to the expression for the threshold voltage above, it is possible to explain the reason why the doping concentration increase causes a reduction in V_{TH} values [8].

$$V_{TH}=V_{FB}-q\times N_D\left[\frac{A}{C_{OX}}+\frac{1}{\varepsilon_{Si}}\left(\frac{A}{P}\right)^2\right]+\frac{\Delta E_0}{q}$$

In the equation, V_{FB}, C_{OX}, A, P, ε_{Si}, ΔE_0 and q represent the flat band voltage, the gate capacitance per unit of length, the cross-section area, the cross-section perimeter, the variation of the minimum level of energy of the conduction band and the electron charge. Once the threshold voltage presents a negative dependence on the charge density, expressed by $-q\times N_D$ in the equation, higher doping

concentrations present higher charge densities and, therefore, lower V_{TH}.

Although simulated results and the V_{TH} calculated by the model present differences, according to Figure 4, considering all the channel lengths studied, the maximum error observed for $N_D=1\times10^{19}cm^{-3}$ is about 24mV and 27mV for $N_D=5\times10^{18}cm^{-3}$, which consist, respectively, 8% and 4% of the simulated threshold voltage. So, it can be concluded that there is a good agreement between the calculated and the simulated results.

The degradation of the V_{TH} with the channel length reduction is due to the reduction of depletion charges controlled by the gate. It leads to a smaller quantity of charge controlled by the gate in shorter transistors in comparison to longer devices and, as a consequence, a degradation of both threshold voltage and subthreshold slope [1].

The results for the subthreshold slope (S) were extracted from the I_{DS} versus V_{GS} results with V_{DS}=50mV, through the inverse of the derivative of the $\log(I_D)$ versus V_{GS} curve, once S is given by the following expression [1]:

$$S=\frac{dV_{GS}}{d\log(I_{DS})}$$

The degradation of the subthreshold slope can be perceived in Figure 5, for L under 80nm.

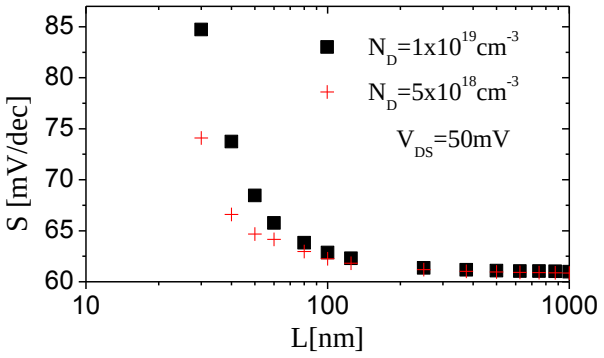

Figure 5 – S versus L results for JNTs with L from 30 to 1000nm, N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$ and V_{DS}=50mV.

From Figure 5, it is observed very similar results and the same trend for both doping concentrations considering the subthreshold slope, which is about 61mV/dec for large channel lengths, when it is not verified any degradation of S. However, there is an increase of the short channel effect for $N_D=1\times10^{19}cm^{-3}$, once S degrades more intensely than for $N_D=5\times10^{18}cm^{-3}$.

The increase of S can be observed directly in the I_{DS} versus V_{GS} curves, considering a logarithmic scale for the current, as shown in Figure 6.

Although both doping concentrations present very close results for subthreshold slope, as shown in Figure 5, from Figure 6 it is observed high differences for the off current (I_{OFF}), which is the drain current value when applied 0V at gate contact. For $N_D=5\times10^{18}cm^{-3}$ the maximum I_{OFF} is about $6.6\times10^{-16}A$ and $5\times10^{-10}A$ for $N_D=1\times10^{19}cm^{-3}$. This increasing of the off current in higher doped concentrations is due to the lower threshold voltage keeping almost the same subthreshold slope.

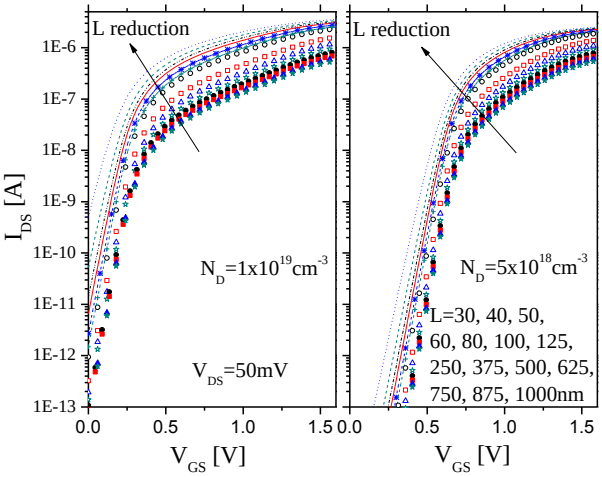

Figure 6 – Logarithmic scale I_{DS} versus V_{GS} curves for JNTs with N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$ and V_{DS}=50mV.

Besides S increasing with L reduction, Figure 6 shows that the off current is higher for shorter devices, which means that this parameter is also affected, in a negative way, when scaling down devices dimensions. It can be noticed that, when turned off, the junctionless device with channel length of 30nm presents a leakage current of $5\times10^{-10}A$, while for a channel length over 125nm the leakage current is lower than $10^{-13}A$, for $N_D=1\times10^{19}cm^{-3}$.

In order to analyze the influence of the high drain to source voltage on the threshold voltage, simulations considering a high electric field at drain region have been performed. So, Figure 7 presents drain current versus gate voltage curves, for the simulated transistors with V_{DS}=1.5V and the same scale for both doping concentrations.

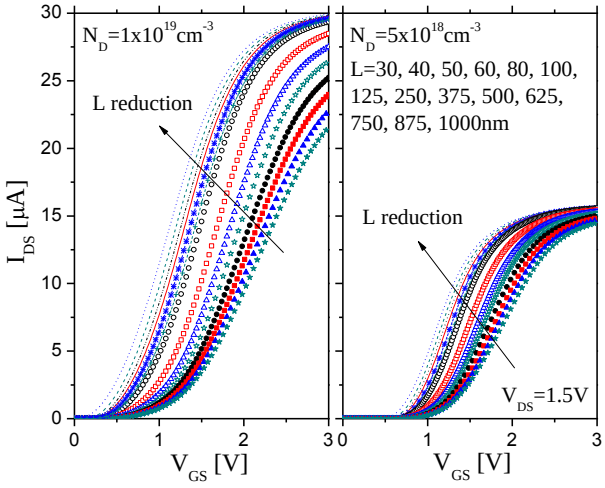

Figure 7 – I_{DS} versus V_{GS} curves for JNTs with L from 30 to 1000nm, N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$ and V_{DS}=1.5V.

Figure 7 shows the same trend of the Figure 3: higher I_{DS} for shorter and more doped devices and degradation due to series resistance.

Once these results were obtained, it was possible to calculate the DIBL (Drain Induced Barrier Lowering), which is an important parameter in short channel devices. It considers the influence of the interaction between the drain and source depletion regions, when applied high drain voltages. In fact, DIBL measures the decreasing of the

threshold voltage due to the reduction of the potential barrier at source region by V_{DS} increase [1].

DIBL was calculated through the following expression, where $V_{TH,1}$ and $V_{TH,2}$ are the threshold voltage for low and high voltage drain, $V_{DS,1}$ and $V_{DS,2}$, respectively [10]:

$$DIBL = \frac{V_{TH,1} - V_{TH,2}}{V_{DS,2} - V_{DS,1}}$$

Moreover, to extract the V_{TH} was used the constant current method, where the threshold voltage is the gate voltage for the drain current described as the following equation [11]:

$$I_{DS} = 10^{-7} \times \frac{(2 \times H + W)}{L}$$

Figure 8 shows DIBL results as a function of the channel length for the simulated junctionless transistors, $V_{DS,1}$ of 50mV and $V_{DS,2}$ equal to 1.5V.

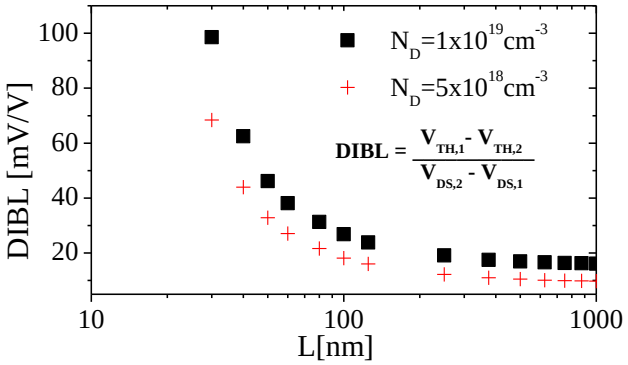

Figure 8 – DIBL versus L results for JNTs with L from 30 to 1000nm, N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$.

From Figure 8, one can note the influence of increasing V_{DS} in the studied junctionless transistors. As expected, once the drain depletion region is more important in shorter devices, they present higher DIBL values, fact which indicates higher variances of the threshold voltage. So, there is a strong increase of DIBL for L from 100nm to 30nm, due to the higher influence of the electric field near the drain. In the worst case, DIBL reaches almost 100mV/V, for L=30nm, in comparison to 16mV/V in the larger junctionless, for $N_D=1\times10^{19}cm^{-3}$.

Moreover, comparing both doping concentrations, for $N_D=1\times10^{19}cm^{-3}$ it is verified higher DIBL values as well as a more pronounced degradation in relation to the less doped transistors. This fact is in agreement with the others results, in which it is observed worsening for the short channel effects considering threshold voltage, subthreshold slope, off current and DIBL degradation for higher doped transistors. This behavior is caused by the increase of the electric field with N_D and, as a consequence, there is an improvement of these undesirable effects [1].

5. CONCLUSIONS

This study has shown the influence of the total channel length reduction on some parameters affected by the short channel effects, considering junctionless nanowire transistors built in SOI substrate with two different doping concentrations.

Considering the studied dimensions for fin width, fin height and gate oxide thickness, investigating threshold voltage, subthreshold voltage, off current and DIBL parameters, it was noted that junctionless devices start to suffer short channel effects with a channel length of 80nm, considering the N_D of $1\times10^{19}cm^{-3}$ and $5\times10^{18}cm^{-3}$.

It was observed that the simulated junctionless nanowire transistors present very good results for the subthreshold slope, considering a channel length longer enough to ensure that the transistor do not suffer short channel effects, once the verified results are around 62mV/dec in comparison to the theoretical limit of 60mV/dec, at room temperature.

Analyzing the off current, it was concluded that it is affected in more than three orders of magnitude for L=30nm, which allows an on drain current over off drain current ratio (I_{ON}/I_{OFF}) of about 10^3A in comparison to the I_{ON}/I_{OFF} of almost 10^6A to the junctionless with total channel length of 125nm, for N_D equal to $1\times10^{19}cm^{-3}$.

Considering the influence of the doping concentration on the operation of the transistors, not only higher N_D leads to higher drain currents, but also brings a worsening in the short channel effects, such as a more pronounced decreasing of the threshold voltage and a sharper increasing of the subthreshold slope, off current and DIBL.

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6. REFERENCES

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