A Comparative Analysis of Two Strategies to Compute BTI Degradation in CMOS Logic Gates

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ABSTRACT
The aging effects are becoming a critical concern in nanometer designs. Bias Temperature Instability (BTI) is one of aging mechanism and causes a shift in transistor threshold voltage (V_{th}), and consequently degradation in circuit performance. Several techniques are presented in the literature to deal with this effect. Usually, two different solutions are explored to compute the V_{th} shift. This paper present a comparison between these two approaches used to compute the device degradation caused by aging effects. The results show that the time under degradation has significant difference, but the BTI behavior reduces this difference in V_{th} and gate delay.

Categories and Subject Descriptors
B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms
Design, Reliability, Performance

Keywords
CMOS, Logic Gates, BTI.

1. INTRODUCTION

CMOS technology has been permanently scaling down during last decades. This scaling enable the significant advance verified in integrated circuit (IC) performance. In the other hand, the continuous scaling emerges several aspects ignored in earlier technologies nodes, as static power, variability, reliability, and radiation effects [1]. The circuit reliability is pointed out as one of the major challenges in nanometer CMOS circuits [2]. Aging mechanisms have become a serious issue to guarantee such reliability during the entire system lifetime. Among several aging mechanisms, Bias Temperature Instability (BTI) is receiving special attention due to its higher severity in nanometer technologies [3].

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The BTI effect acts in CMOS transistors when they are in a steady state condition. The effect is also divided in two phases: stress and recovery. These two phases are well modeled in short terms models [4]. In long term analysis, the computational cost required for short term models make the use of those models an impracticable alternative. Long terms models are developed to reduce the computational complexity [5-6]. Those models explore the signal probabilities to compute the stress and recovery phases associated to BTI effect.

Two approaches are used in the literature to deal to long term analysis. The first one considers just the gate signal probability (SP) [5]. The second one claims to represent more precisely the real degradation conditions exploring the gate signal probability associated to the transistor arrangement to compute the transistor stress probability (TSP) [6]. It is well established that TSP approach provides more accurate result at a higher computational cost. However, a comparative analysis in logic gate delay has not been investigated between both solutions. This work compares the difference in logic gate delay degradation when SP and TSP approaches are applied to compute BTI delay degradation in CMOS logic gates.

The follow text is organized as follow. Section 2 presents a brief review related to BTI mechanism and analytical models. A case study to illustrate the differences explored in this work is presented in Section 3. Section 4 describes the used methodology and simulation results are presented in Section 5. Finally, conclusions are presented in Section 6.

2. BACKGROUND

Bias temperature instability (BTI) is a degradation phenomenon investigated since the late 1960s. Even though the exact degradation causes are not well understood yet, it is now commonly admitted that under a constant gate voltage bias and elevated temperature a built up of interface traps and charges occur both at the oxide-substrate interface and in the oxide layer [4]. This situation is usually named stress phase. When that constant gate voltage bias is removed, some traps are recovered, reducing the device degradation. This case is known as recovery phase.

This effect was usually associated to PMOS devices (negative bias temperature instability – NBTI). Due to high-κ metal gate used in newer technologies, PBTI (positive bias temperature instability) on NMOS devices is also becoming an important aging concern

[4]. The effect increases the transistor threshold voltage (V_{th}), so reducing the circuit speed [2].

As mentioned early, models that compute stress and recovery phases have elevated computational cost. The long term degradation in transistor threshold voltage is usually computed considering the gate signal probability. For specific technology node and a given set of environmental conditions, the $\Delta V_{th\_BTI\_SP}$ can be expressed by the following equation [7]:

$$\Delta V_{th\_BTI\_SP} = a \,.\, (SP \,.\, t)^n \qquad (1)$$

where a is a technology dependent constant, t is time, and n is the NBTI time exponential constant. SP is the gate voltage signal probability. For PMOS transistor, the interest signal probability is when voltage is '0', while for NMOS transistor when voltage is 'Vdd'.

In TSP approach, the degradation is computed considering the gate and source voltage bias. The main reason for this extension is the fact that the BTI degradation is associated to the elevated electric field across the transistor gate structure. From this statement, the maximum electric field is only experience when the the gate-to-source voltage is Vgs = –Vdd and Vgs = Vdd, for PMOS and NMOS, respectively. For specific technology node and a given set of environmental conditions, the $\Delta V_{th\_BTI\_TSP}$ can be expressed by the following equation, as a function of the transistor stress probability (TSP) [6]:

$$\Delta V_{th\_BTI\_TSP} = a \,.\, (TSP \,.\, t)^n \qquad (2)$$

where a is a technology dependent constant, t is time, and n is the NBTI time exponential constant. TSP is the probability of PMOS transistor is negative biased and NMOS transistor is positive biased. It is a function of the input signal probability and the position of the transistor in the network arrangement [6].

3. SP VERSUS TSP EXAMPLE

It is well stabelished that the transistor arrangement of a logic gate has impact in its area, performance, and power consumption. This section explores of the transistor network influence in aging degradation. The AOI21 logic gate, illustrated in Figure 1, is used to exemplify the differences in analysis that evaluates the device degradation due to aging effects.

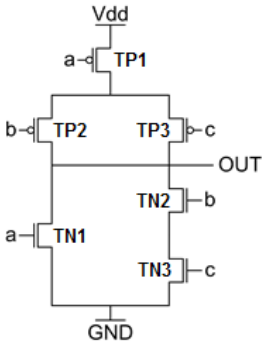

Figure 1. AOI21 gate with description of transistors.

As discussed early, there are two methodologies commonly used to compute the device degradation. There is one that compute the transistor degradation considering only the gate signal probability (SP). The other one explore the voltage bias in all transistors terminals, associating the gate signal probability to the transistor arrangement to provide the transistor stress probability (TSP). The difference in btoh approaches are the time that the device is under stress condition.

Table 1 illustrates this time under stress degradation through the probabilities computed by previous approaches: SP and TSP. The values where calculated considering a equal probability os 0.5 for all input signal. SP analysis takes into account only the probability of the signal reaching the transistor gate, and consequently all devices have the same degradation probability. On the other hand, the TSP analysis considers the steady state of all transistor terminals to characterize the transistor stress condition. This steady state is obtained from gate signal probabilities and transistor arrangement [6]. The differences when TSP degradation is considered are verified in transistors that are not connected to the power rails. In other words, the difference is observed in series transistors arrangements. In the simple AOI21 example, some devices (TP2 and TP3) experience only half of degradation when both approaches are compared.

Table 1. Probability of signal analysis in relation to SP and TSP for each transistor.

Transistor	(SP)	(TSP)
TP1	0.5	0.5
TP2	0.5	0.25
TP3	0.5	0.25
TN1	0.5	0.5
TN2	0.5	0.375
TN3	0.5	0.5

METODOLOGY

The methodology used to compare both device degradation solutions consist in compute the SP and TSP values in several logic gates illustrated in Figure 2. These SP and TSP values are used in equations (1) and (2) to obtain the V_{th} shift of each device. These data is applied in 'Vth0' parameter of transistor model card and electrical simulations are performed to compute the logic gate delay degradation.

The logic gates illustrated in Figure 2 are described as spice netlist using a 32nm predictive technology [8]. Each one of these logic gates has three versions. The first one is named "fresh" and consists in original version of each logic gate. The second one is called "sp" and consists in a version with degraded devices according to SP degradation. The third one is the "tsp" and it is a description with degraded transistor according to TSP devices. Each version of logic gates is computed by and electrical characterization tool [9].

4. SIMULATION RESULTS

A summary of simulation results is presented in Table 2, 3, and 4. To simplify the discussion, the SP and TSP acronyms are used to represent both approaches discussed in this work. The models that compute de Vth degradation consider a maximum V_{th} degradation of 50mV for SP = TSP = 1 and the BTI behavior follow a power law with n=1/6 [7].

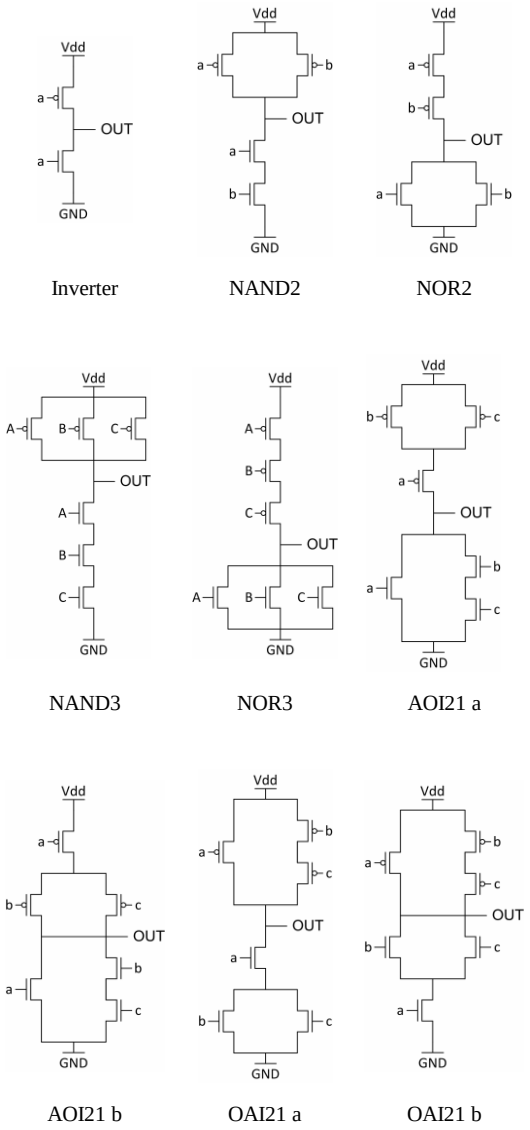

Figure 2. CMOS logic gates used to compare two device degradation solutions.

Table 2 presents the average probability of transistor been in stress conditions according to SP and TSP approaches. As discussed in Section 3, the influence of transistor arrangement achieves in average difference in degradation values up to 20%. This difference achieved the higher values in larger transistor series association and also in gate with less devices connected to the power rails, as verified in NAND3 and AOI21 b.

Table 3 presents the average V_{th} shift for each logic gate. Different from data presented in Table 2, the difference between SP and TSP degradation procedures are not so large. This behavior can be explained by the power law (with n=1/6) behavior presented in equations (1) and (2).

Finally, the gate delay degradation for the two approaches are presented in Table 4. As expected, the gate delay follows the behavior verified in V_{th} shift analysis and presents in an average degradation difference up to 7.3%.

Table 2. Average probability of transistors stress conditions for SP and TSP approaches .

Logic Gate	Average Device Degradation Probability		Difference (%)
	SP	TSP	
INV	0.5	0.50	0
NAND2	0.5	0.44	12
NAND3	0.5	0.44	12
NOR2	0.5	0.40	20
NOR3	0.5	0.40	20
AOI21 a	0.5	0.46	8
AOI21 b	0.5	0.40	20
OAI21 a	0.5	0.46	8
OAI21 b	0.5	0.40	20

Table 3. Average Vth shift according to SP and TSP approaches.

Logic Gate	Average V_{th} Shift (mV)		Difference (%)
	SP	TSP	
INV	46	46	0
NAND2	46	45	2.2
NAND3	46	45	2.2
NOR2	46	43	6.5
NOR3	46	43	6.5
AOI21 a	46	45	2.2
AOI21 b	46	44	4.3
OAI21 a	46	45	2.2
OAI21 b	46	44	4.3

Table 4. Gate delay degradation according to SP and TSP solutions.

Logic Gate	Average Gate Delay Degradation (%)		Difference (%)
	SP	TSP	
INV	11.3	11.3	0
NAND2	11.0	10.6	3.6
NAND3	11.0	10.6	3.6
NOR2	11.2	10.5	6.3
NOR3	11.0	10.2	7.3
AOI21 a	11.7	11.4	2.6
AOI21 b	11.3	10.9	3.5
OAI21 a	11.1	10.9	1.8
OAI21 b	11.2	10.7	4.5

5. CONCLUSION

This work presents a comparative analysis of two approaches that are used to compute de transistor degradation due to aging effect. The analysis has shown that the time under degradation of a specific devices can achieve significant values, but this large difference is not reflected in Vth shift and consequently in gate delay degradation. This comportment is consequence of BTI power law (n=1/6) behavior.

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