Influence of Ground-Plane Doping on Bulk FinFET

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ABSTRACT

This paper studies the influence of ground-plane doping concentration on bulk FinFET characteristics. The bulk FinFET structure normally presents a doping region under-the channel (ground-plane) in order to avoid drain parasitic conduction current. The influence of the ground-plane concentration value were studied through 3D numerical simulations. As we scale from lower to higher doping layer, it was observed a shift on the threshold voltage and a decrease of maximum transconductance in response of the decrease of mobility. A more steep subthreshold inclination, meaning a better control over the current from the gate is also observed for higher doping layer.

Keywords

Bulk FinFET, multiple-gate devices (MuGFET).

1. INTRODUCTION

In 1960 Gordon Moore predicted that with the technological advance the number of transistors in a chip would increase [1] (Moore's law indicates the number would double every two years) so to keep this pace, came the need to smaller transistor, lead to the rising of new devices as alternatives in order to maintain and increase the performance of the devices, as we scale them down.

The FET (field Effect Transistor) had been a successful industrial dispositive, and the CMOS technology is today the main technology in the electronic industry. It consists in a transistor with an isolation oxide layer (SiO2) between the gate electrode and the Si-bulk wafer. In time the SOI (silicon on insulator), a MOSFET device with a silicon layer below the channel technology took place as an alternative for some unwanted as parasitic and short-channel effects.

Then came the multiple-gate devices with a better performance, and advantages in several parameters as electrostatic integrity and DIBL (Drain Induced Barrier Lowering). One example of MuGFET is a triple-gate nMOSFET also called bulk FinFET [2] device with a gate around three sides, is shown on figure 1.

The aim of this work is to better understand the bulk FinFET transistor behavior based on three-dimensional simulations. These simulations were performed using Atlas from Silvaco.

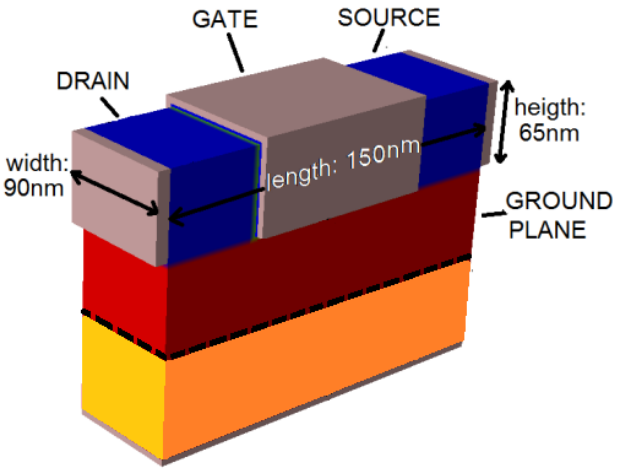

Figure 1. Schematic of a bulk FinFET transistor.

2. DEVICES

The studied devices are vertical triple-gate nMOSFETs constructed on bulk silicon substrate. All the devices have the following characteristics: a gate oxide thickness of 2nm, channel length of 150nm, width of 90nm, height of 65nm and body depth of 210nm. The channel has a natural wafer doping ($1x10^{15}cm^{-3}$), and the drain and source have a doping of $1x10^{20}cm^{-3}$. It was also implemented an n-type lightly doped region (LDD structure) of $1x10^{18}$ atom/cm^{-3}, aiming to improve the devices performance.

Besides that, it was also simulated two different structures: a standard silicon substrate (bulk), and a device with a higher doped layer, in the region below the channel (GP - Ground Plane). The second structure was also simulated with two different GP doping concentrations: $1x10^{17}cm^{-3}$ and $3x10^{18}cm^{-3}$.

In the simulations it was used the mobility model that accounted the carriers concentration, the vertical electric field, temperature, the transversal electric field and the SRH models

3. RESULTS AND ANALYSIS

Figure 2 shows the current density for each device. It is possible to notice a total current density reduction as the doping below the channel (GP) increases. The higher concentration leads to the turn off the parasitic transistor resulting in a leakage current reduction. Therefore, a better control of the gate over the drain current is obtained as well as a better relation between ON and OFF-state currents (I_{ON}/I_{OFF}).

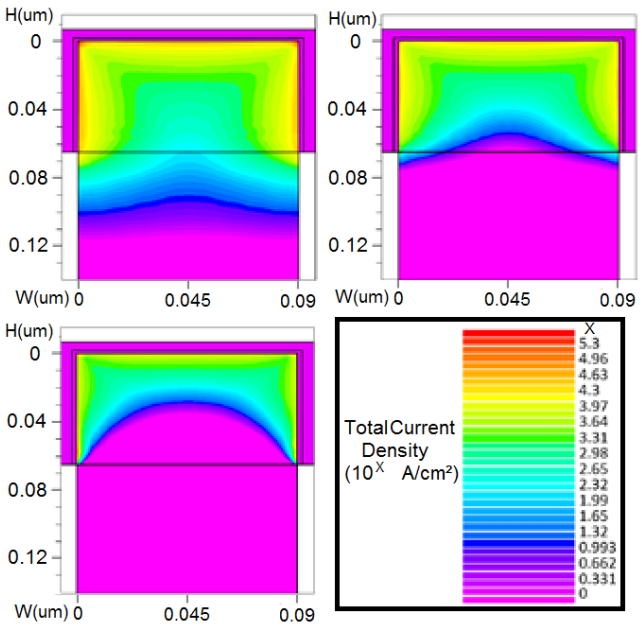

Figure 2 Total current density of a bulk FinFET with ground-plane doping of .A) 1x10^{15}cm^{-3}, B) 1x10^{17}cm^{-3}, C) 3x10^{18}cm^{-3}.

Figure 3 presents the drain current (I_{DS}) as a function of gate voltage (V_{GS}) for all analyzed structures. When drain current is plotted in a linear scale, it is observed a shift of the total drain current toward to a higher gate voltage for devices with additional doping layer. The reduction of drain current as GP doping concentration increases due to the high-low junction below the channel. The depletion from the high doped region (GP) to the channel precludes the current to flow near to this region, shifting the current density to the surface direction. However, when I_{DS} is plotted in a logarithmic (figure 4) an improvement of the SS behavior is also observed for a device with a higher doped layer.

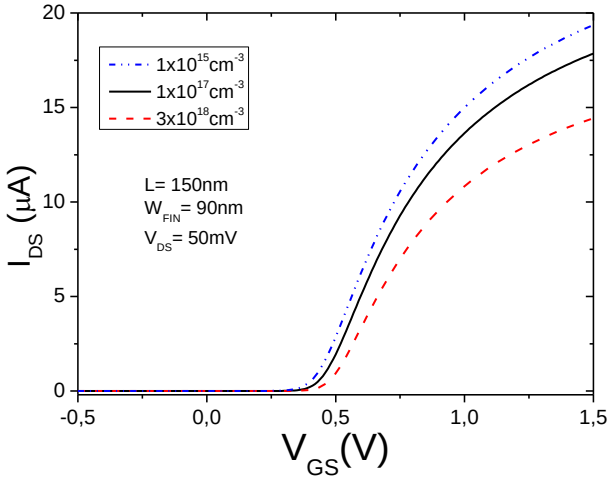

Figure 3. Drain current as a function of gate voltage for different ground-plane concentrations.

Both effects (better SS behavior and the drain current shift) are explained by the parasitic conduction turn off. The shift of the threshold voltage to higher gate voltages as the doping concentration increase is observed in figure 5. Since the threshold voltage (Vth) was extracted using the second derivative method [3], the obtained Vth for bulk FinFET device includes the leakage conduction. However, when this component is turned off, the Vth is only related to the main conduction, near to the Si/SiO_2 interface, which requires a higher gate voltage to invert the channel.

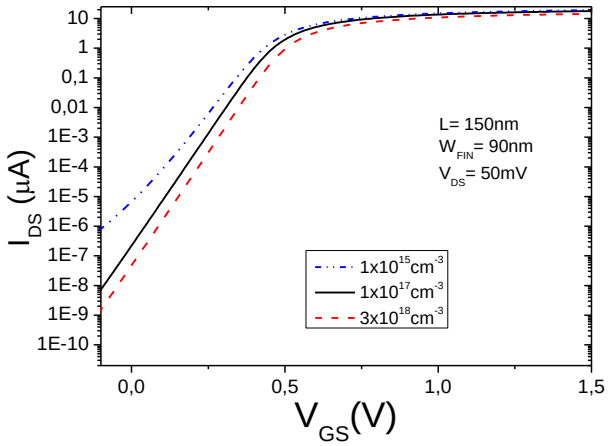

Figure 4. Drain current as a function of gate voltage for different ground-plane concentrations.

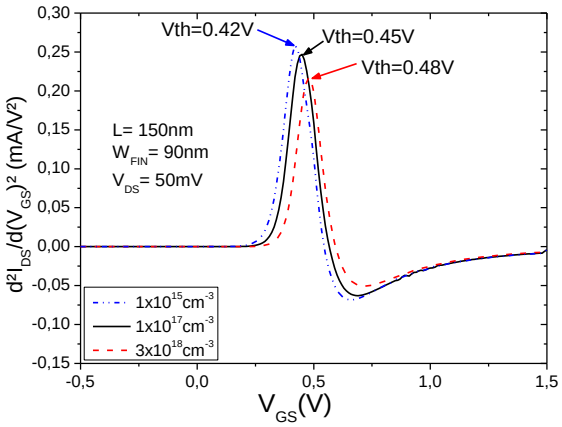

Figure 5. Second derivation of drain current as a function of gate voltage for different ground-plane concentrations.

The transconductance shown in Figure 6, were obtained from the first derivation of drain current and reflects the transistor capability of controlling the drain current through gate voltage. A higher transconductance is expected as you use the layer, because the current flow occurs more concentrated closer to the gate, however, it's observed a decrease of the maximum of transconductance, as a consequence of a mobility degradation caused by the confinement of the current and the electric field.

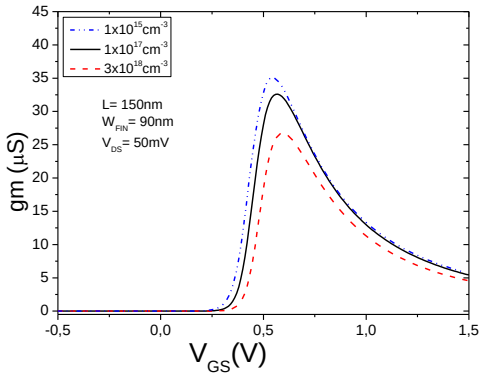

Figure 6. Transconductance for different ground-plane concentration.

The subthreshold slope represents how the increase of V_{GS} affects the current, in other words, a low SS means a small increase of gate voltage can generate a great increase of drain current. In order to quantify the subthreshold slopes (SS) improve, the SS values were extracted from the expression:

$$SS = {d(Vgs)}/{d(\log(Ids))} \quad (1)$$

The extracted values were show in figure 6.

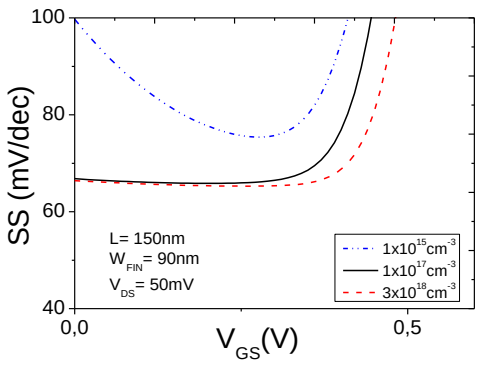

Figure 7. Subthreshold slope for different ground-plane concentration.

To a easier comparison of all the results, the main parameters are shown in table 1.

Table 1. Comparison of transconductance and SS.

Ground-Plane concentration	Maximum Transconductance (µS)	Subthreshold Slope (mV/dec)
$1x10^{15}cm^{-3}$	35.10	75
$1x10^{17}cm^{-3}$	32.60	66
$3x10^{18}cm^{-3}$	26.74	65

Taking the standard devices as a reference, the obtained SS values indicates an improvement of 12% with the implantation of the doped layer of $1x10^{17}cm^{-3}$ and 13.3% for a layer of $3x10^{18}\,cm^{-3}$.

In table 2 are presented a few other parameters also taken into account as the relation I_{ON}/I_{OFF} and the drain-induced barrier lowering (DIBL), obtained from the expression:

$$DIBL = \frac{[Vth(Vds{=}50mV) - Vth(Vds{=}1.2V)]}{(1.2-0.05)} \quad (2)$$

The currents I_{ON} and I_{OFF} were measured in the I_{DS}-V_{GS} curves in the points V_{TH} + 0,5V for I_{ON} and V_{TH} - 0,5V for I_{OFF}. The results show a decrease in both currents, also as consequence the leakage current decrease, but an increase of the relation as I_{OFF} scale down faster than I_{ON}. As the devices scale down a few effects have to be consider, like the short-channel effects (SCE) that represents effects that interfere in the gate control due to the channel size. The DIBL is one of those effects, and it represents the drain voltage influence over the threshold voltage. The influence, as it is shown in the table values, becomes smaller in higher doping concentrations, to a point of been considered insignificant (lower than 20mV/V).

Table 2. Comparison of the I_{ON}/I_{OFF} and DIBL.

Ground-Plane concentration	I_{ON} (µA)	I_{OFF} (pA)	I_{ON}/I_{OFF} ($x10^6$)	DIBL (mV/V)
$1x10^{15}cm^{-3}$	66.62	57.06	1.17	52
$1x10^{17}cm^{-3}$	65.69	0.216	304	35
$3x10^{18}cm^{-3}$	55.73	0.117	476	17

4. CONCLUSIONS

This paper studied the influence of the ground-plane doping concentration on the main bulk FinFET devices. The use of different body doping concentrations in a bulk FinFET device show a decreasing of the leakage current below the channel when the doping increases. It caused the threshold voltage shifting to higher values due to increase of channel effective doping. Even though, the device had a loss in maximum transconductance, due to a stronger electric field mobility degradation, it presented a more efficient control over the drain flow in subthreshold region (lower SS value).

5. ACKNOWLEDGMENTS

The authors would like to thank the University of São Paulo for the financial support to this work.

6. REFERENCES

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