Design of an ASK Demodulator and a Bandgap Reference for a Passive RFID Tag for 13,56MHz

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ABSTRACT
A passive radio-frequency identification (RFID) tag system is proposed in this work. The amplitude shift keying (ASK) demodulator and the bandgap voltage reference were sent for fabrication using 0.18um TSMC technology. Some topologies are proposed for the other blocks that compound the system.

Keywords
RFID;CMOS;ASK;Bandgap.

1. INTRODUCTION
Technologies using RFID have been extensively used nowadays, aiming the time reduction for the data acquisition. RFID is a generic expression used to describe the wireless transmission of an identity number assigned to an object or a person.

A typical RFID tag is compounded by a chip connected to an antenna, which can allow the wireless transmission of its identity number to a reader. The chip can store up to 2KB of data, which is sufficient to describe information about a product, as fabrication date and destination.

To read the information stored in a RFID tag is necessary a device, called reader, adapted of one or multiples antennas able to transmit and receive information from the tag and send the result of this communication to a computer.

The tag can be passive or active. The passive tag doesn't use a voltage source. It uses the electromagnetic waves, sent by the reader, to generate the energy necessary to make the circuit work. The active tag uses a battery to energize the chip and to transmit the information for the reader.

In the present paper, a passive RFID tag will be proposed. Some internal blocks were designed and sent for fabrication using the 0.18um/CMOS TSMC technology.

2. PROPOSED CIRCUIT
The block diagram of the proposed passive RFID tag is presented in Fig. 1. The system is composed by the following blocks:

Rectifier – The RF signal received by the antenna is rectified to generate the needed DC voltage to supply the other blocks. Therefore, this block uses a charge pump and a low-dropout regulator (LDO regulator) to execute this procedure. A bandgap circuit is also used to provide a reference voltage and to compensate the temperature effects.

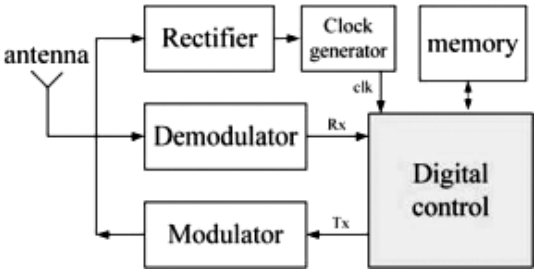

Fig. 1 – RFID Analog Front End Block Diagram [1].

Demodulator – The proposed circuit accomplishes an ASK demodulation. It was designed using schottky diodes and a hysteresis comparator with a temperature compensated current source.

Clock Generator – It is the internal oscillator, responsible to provide the necessary clock for digital circuitry. It uses a traditional ring oscillator.

Modulator – The proposed architecture uses backscatter techniques to provide the tag's ID through BPSK modulation.

In this paper it will be shown the design of an ASK demodulator and a bandgap voltage reference. These blocks were sent for fabrication using the 0.18um/CMOS TSMC technology. Moreover, the rectifier, clock generator and modulator will be discussed through a brief theoretical review, where some architectures will be proposed.

3. BUILDING BLOCKS
3.1 Low-dropout Regulator
Low dropout regulators are an inexpensive and simple way to build a voltage source with no compensation capacitor on its output, resulting in a smaller circuit [2]. Power management is very important in integrated circuits due to the limited available energy and it is critical in autonomous devices. This way, power rectifier circuits have a big role in passive RFID systems [3], generating a stable voltage, with low power consumption and high efficiency, thanks to a small difference between input and output voltages [4].

The basic topology used and proposed to build the LDO regulator is shown in Fig. 2. It consists of a high gain operational amplifier which is used as an error amplifier [5]. The pass transistor (Mp) must be carefully designed so that it can be able to provide the power requested by the circuit. The voltage reference Vref is obtained by a bandgap reference.

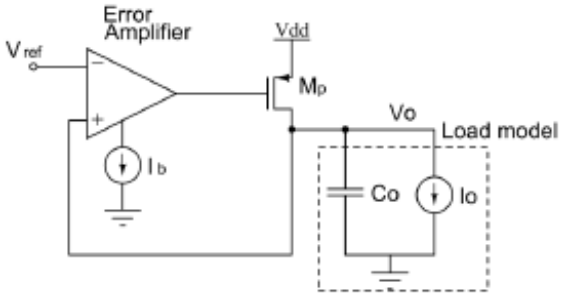

Fig. 2 – LDO regulator proposed topology.

3.2 Bandgap Reference

The bandgap main purpose is to generate a voltage reference that has as minimum dependence with temperature [6]. This can be made when two voltages, with different and opposite signs temperature coefficients (TC), are joined. As a result, they cancel each other, generating a voltage reference with low temperature dependence [7].

The schematic of the bandgap, made using CADENCE Virtuoso software, is presented in Fig. 3. It is composed by an operational amplifier (OP), an output buffer, bipolar transistors and a resistive voltage divider. Equation (1) rules the bandgap behavior, where VBE is the base emitter voltage of transistor Q4 and VT is the thermodynamic voltage (approximately 25mV at 25^0C).

$$V_{REF} = V_{BE4} + V_T \ln(n)(1 + R_1/R_3) \quad (1)$$

The power consumption is 38.77µW, using a supply voltage of 1.8V. It has two outputs, the first with 1.22 V and the second one with 613 mV and these values are stable in a range of -30ºC to 130 ºC (Fig. 4).

3.3 Charge Pump

The charge pump is a circuit that can generate an output voltage larger than the supply voltage. This can be made by a capacitor network providing a voltage gain per stage. As the charge pump is built using many stages as the application requires, the voltage sum of all the stages provide the final DC voltage. This kind of circuit has many applications, such as nonvolatile memories EEPROM, which is used in RFID tag memory, DC-DC converters and power management chips [8]. Some advantages are: high energy efficiency, low power consumption, small area and low current drivability, being independent of the number of multiplier stages [9].

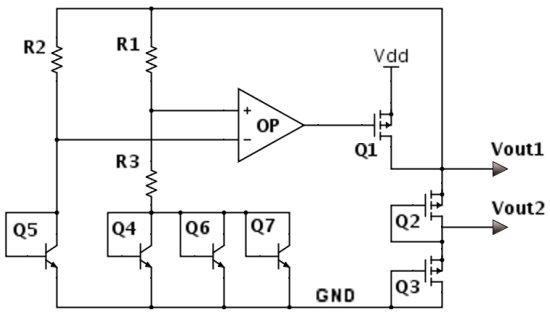

Fig. 3 – Schematic of the bandgap.

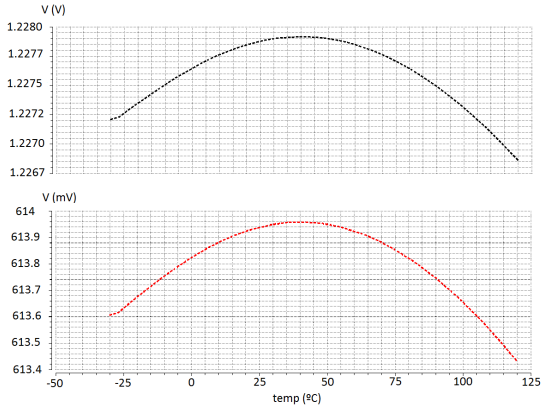

Fig. 4 – Bandgap simulation results using a constant load.

The charge pump works charging and discharging capacitances to transfer energy to the output [10].

The most famous architecture is the Dickson charge pump (Fig. 5). Its gain depends on the numbers of stages. Its operation is simple. It uses two clocks in antiphase driving switches, that charge and discharge individual cells composed by a diode and a capacitor, during each half of clock cycle.

3.4 ASK Demodulator

The proposed ASK demodulator uses an envelope detector, an average filter and a hysteresis comparator to provide binary values in its output. Its schematic is shown in Fig. 6.

The envelope detector uses a Dickson voltage multiplier. Besides, schottky diodes are used due to their low forward voltage drop.

After the envelope detector the peak voltage is approximately 600mV.

The average voltage is obtained using a low pass RC filter. The low cutoff frequency demands the use of a large resistor. As a result, a transistor biased in the active region is used to provide the required resistance.

A hysteresis comparator is used to compare the envelope signal with the average voltage. Its schematic is shown in Fig. 7. This kind of circuit was chosen to make the comparison more resistant to ripples which could interfere in the comparison. The circuit consumes 5 µA using a voltage supply of 1.8V.

The circuit simulation is shown in Fig. 8. The curves presented are, from the top to the bottom, the ASK signal, the envelop signal, the average voltage and the comparison result.

The power consumption is 9uW. The circuit was simulated in temperature, which resulted in a working range of -15ºC to 95ºC. The entire demodulator occupies approximately 270,8µm x 185µm.

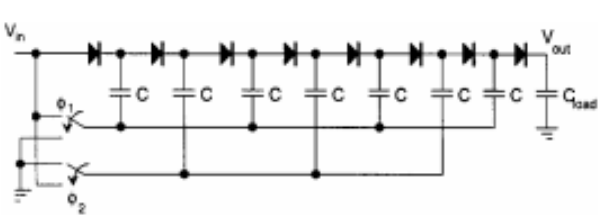

Fig. 5 – Dickson charge pump.

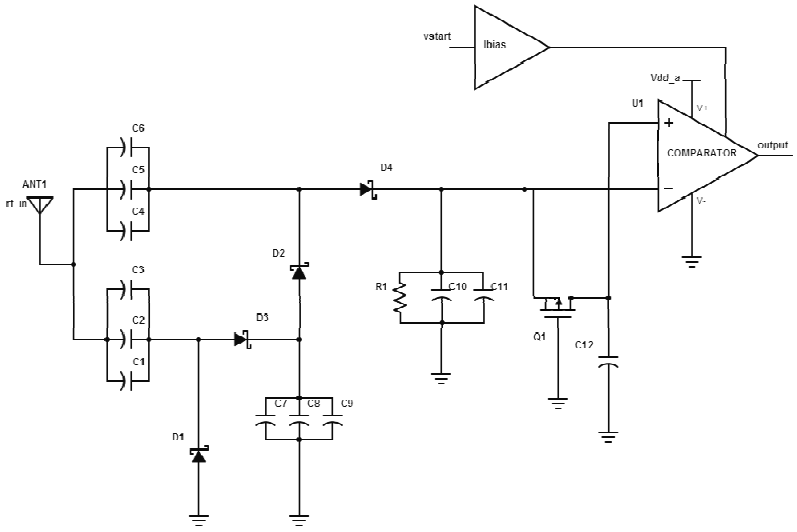

Fig. 6 – ASK Demodulator.

3.5 BPSK Modulator

The tag transmits data to the reader using BPSK modulation through backscatter process. This kind of modulation is accomplished modifying the impedance of the tag's antenna. This procedure results in the reflection of part of the signal transmitted by the reader. The reader senses the reflected signal which is modulated in phase (BPSK).

Figure 9 shows the modulation process. It uses a transistor to switch the impedance between two values.

3.6 Clock Generator

The proposed circuit uses a ring oscillator to provide the necessary clock.

The period of oscillation is determined by the topology and some parameters of the manufacturing process. The circuit is composed by an odd number of inverters in series, where the output of the last inverter is connected to the input of the first.

The odd number of inverters causes the circuit to have no stable operating point, producing the oscillation. The period of oscillation (T) can be obtained by the propagation time of the signal through the inverter. Equation (2) can be used to calculate the oscillation period.

$$T = 2*Tp*N \quad (2)$$

Tp is the propagation time of a single inverter and N is the number of inverters.

To adjust the output frequency some methods can be applied, such as the use of different number of inverters, change the supply voltage, change the output capacitance and modify the current biasing the circuit.

4. CONCLUSION

The ASK demodulator and the bandgap voltage reference were

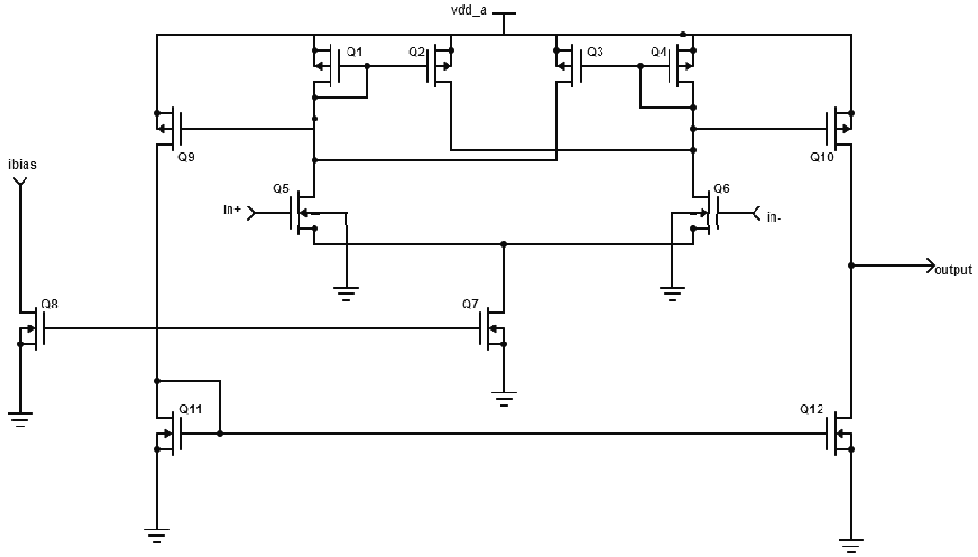

Fig. 7 – Hysteresis Comparator.

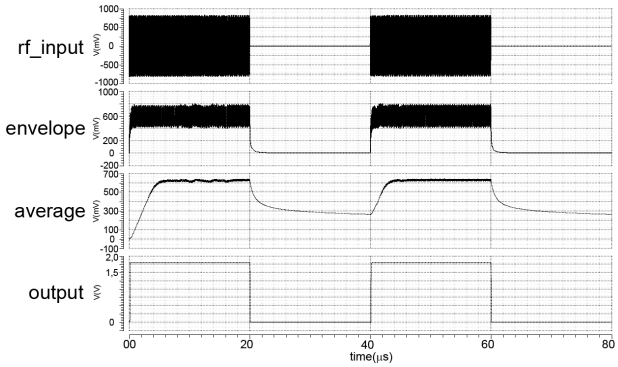

Fig. 8 – Transient Simulation.

sent for fabrication using 0.18um TSMC technology. The system will be completed modeled using Verilog-AMS language and, after characterize the ASK demodulator and bandgap voltage reference in laboratory, mixed signal simulation will be used to verify whether the proposed system accomplish the needed functionality.

5. ACKNOWLEDGMENT

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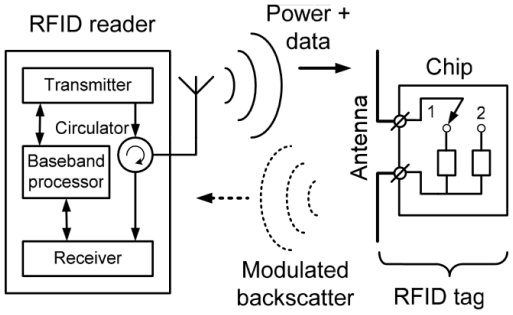

Fig. 9 – Backscatter Modulation [11].